


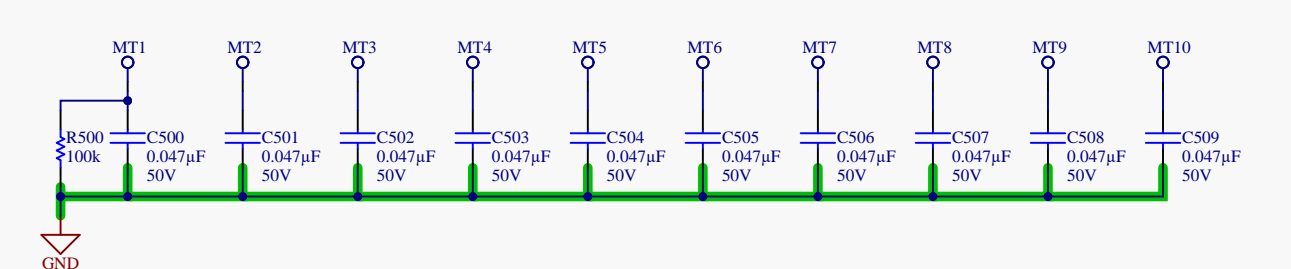
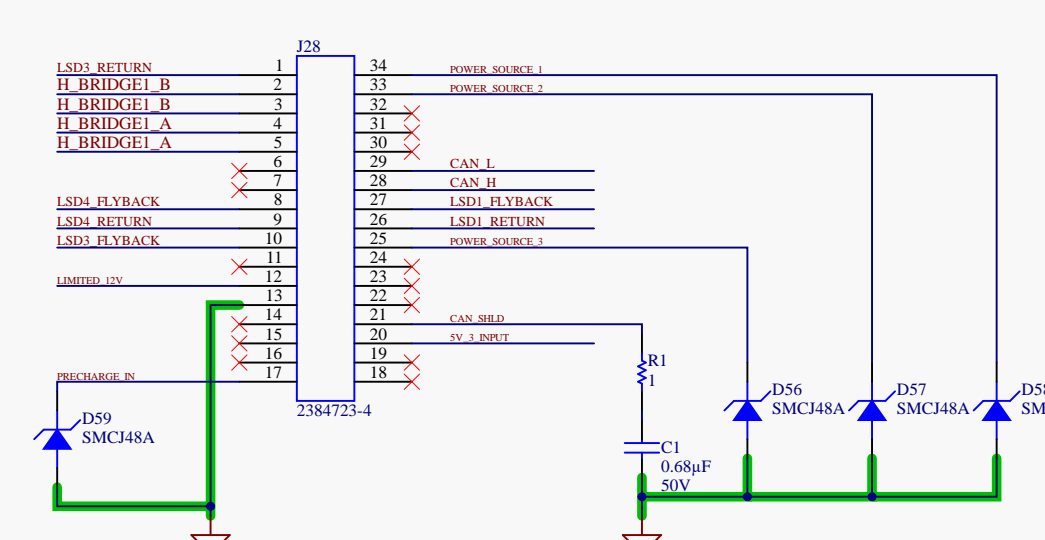
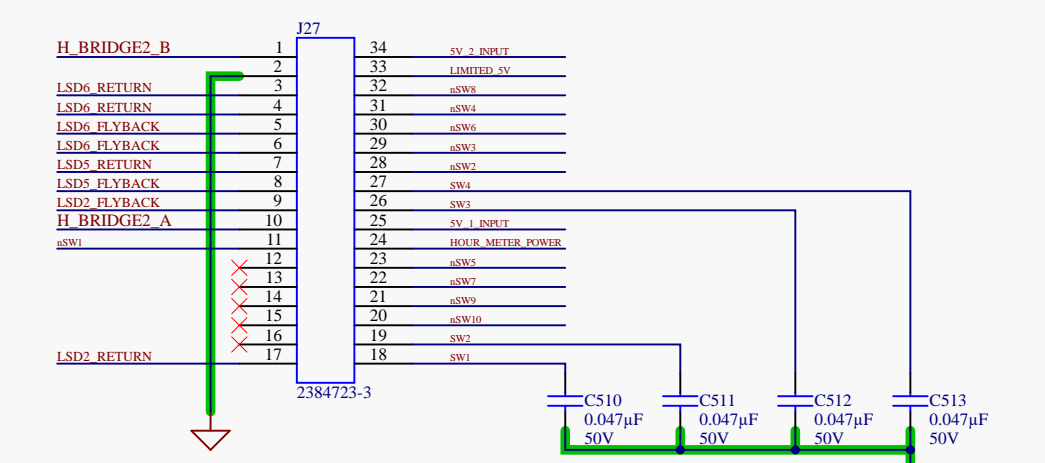
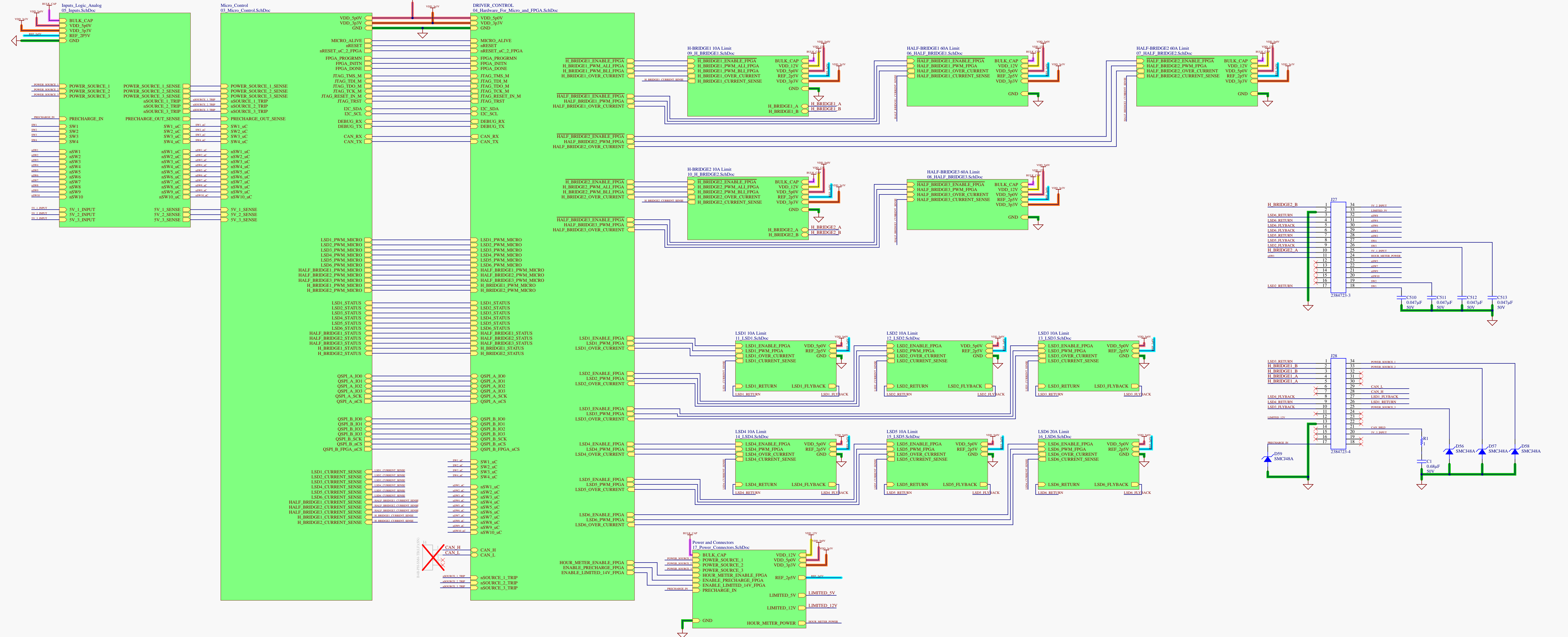
SATURN SERIES TBR3206 MACHINE CONTROLLER

Changelog:
 REV D:
 Updated name and title of documents to reflect new component name.
 Page 3 -
 I2C Bus Pullup Correction: R405 R406 -> 2.74k. Fixed pullup strength for acceptable logic levels.
 FPGA Programming Pin Correction: R126 R127 R128 -> 100k. Decreased strength of FPGA programming pins to account for FPGA pull-ups during programming.
 HW Revision Bit Resistors updated to 3 // 0x011
 Page 9 -
 H-Bridge 1 Current Sense Fix: R211 -> 3mOhm. Resolved scenario where overcurrent conditions on H-Bridge 1 could damage uC.
 Page 17-
 Precharge timing correction: C475 -> 4.7uF, R436 R439 -> 23.7k. Reduced rate of precharge to meet 1.5A requirement.

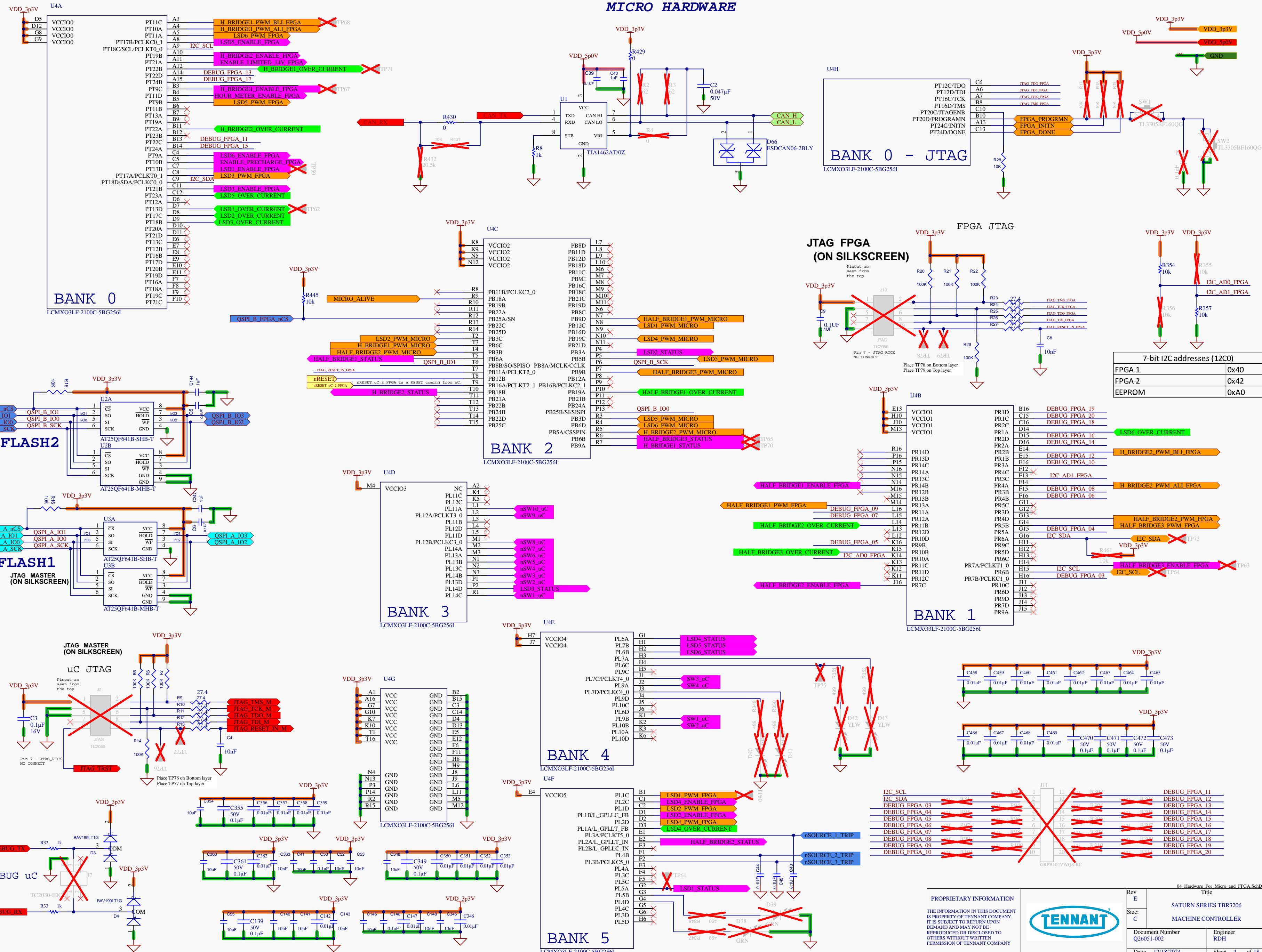
REV E:
 Page 4: Updated HW Rev Bits to 4
 Pages 9-15: Replaced 0.033uF caps on gates of FETs with 10k resistors to eliminate ringing that was causing component damage.

PCB ○ Q25099-002

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		Size:	MACHINE CONTROLLER	
		B	Document Number	Engineer
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		Date: 12/18/2024	Sheet 1 of 18	



MICRO HARDWARE



BANK 0 - JTAG
LCMXO3LF-2100C-5BG256I

JTAG FPGA (ON SILKSCREEN)

7-bit I2C addresses (12C0)	
FPGA 1	0x40
FPGA 2	0x42
EEPROM	0xA0

FLASH2

FLASH1
JTAG MASTER (ON SILKSCREEN)

JTAG MASTER (ON SILKSCREEN)
uC JTAG

DEBUG uC

BANK 2
LCMXO3LF-2100C-5BG256I

BANK 3
LCMXO3LF-2100C-5BG256I

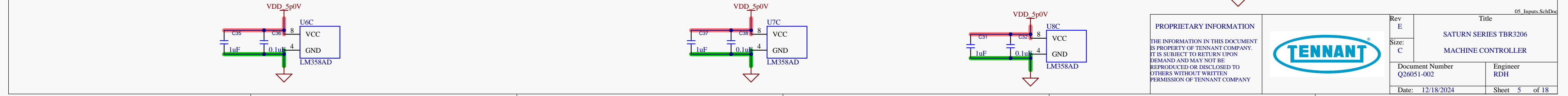
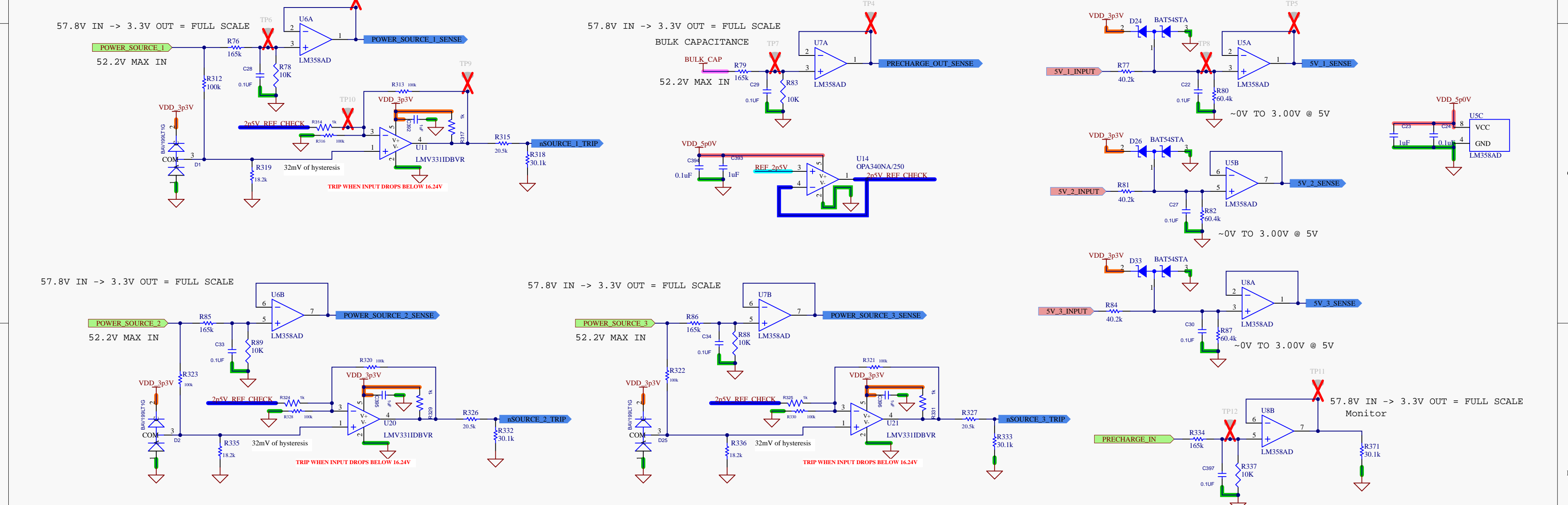
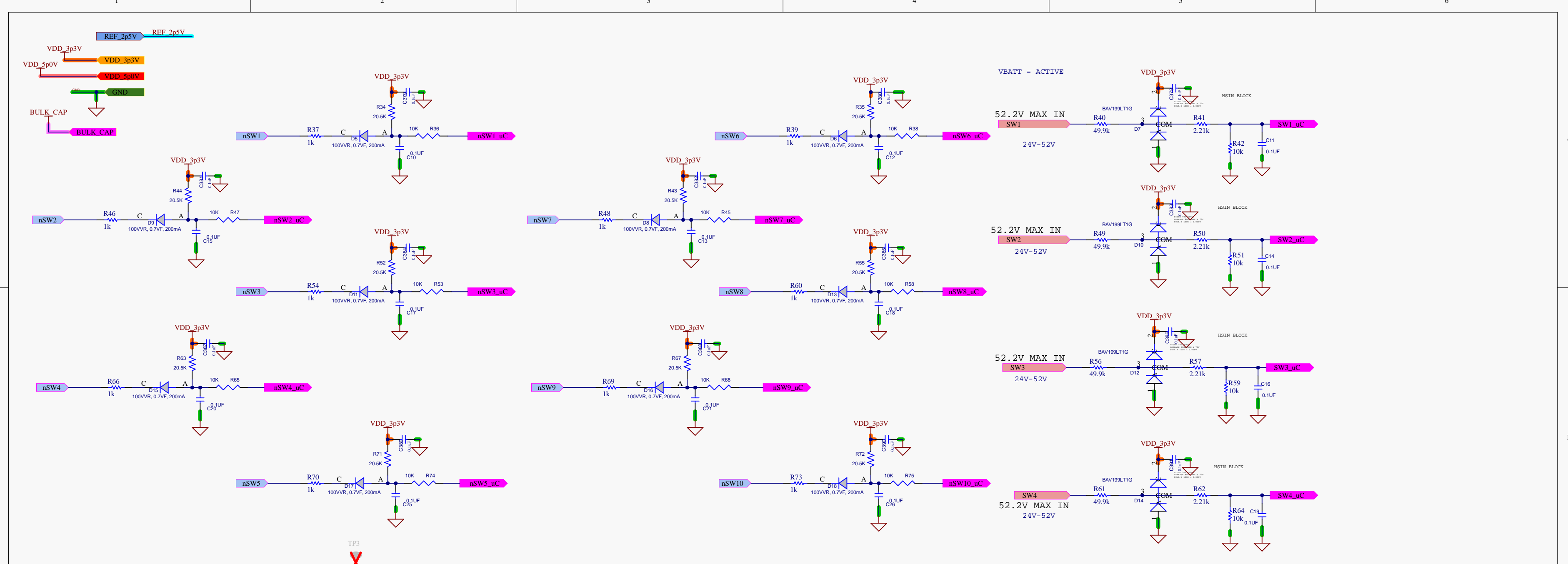
BANK 4
LCMXO3LF-2100C-5BG256I

BANK 5
LCMXO3LF-2100C-5BG256I

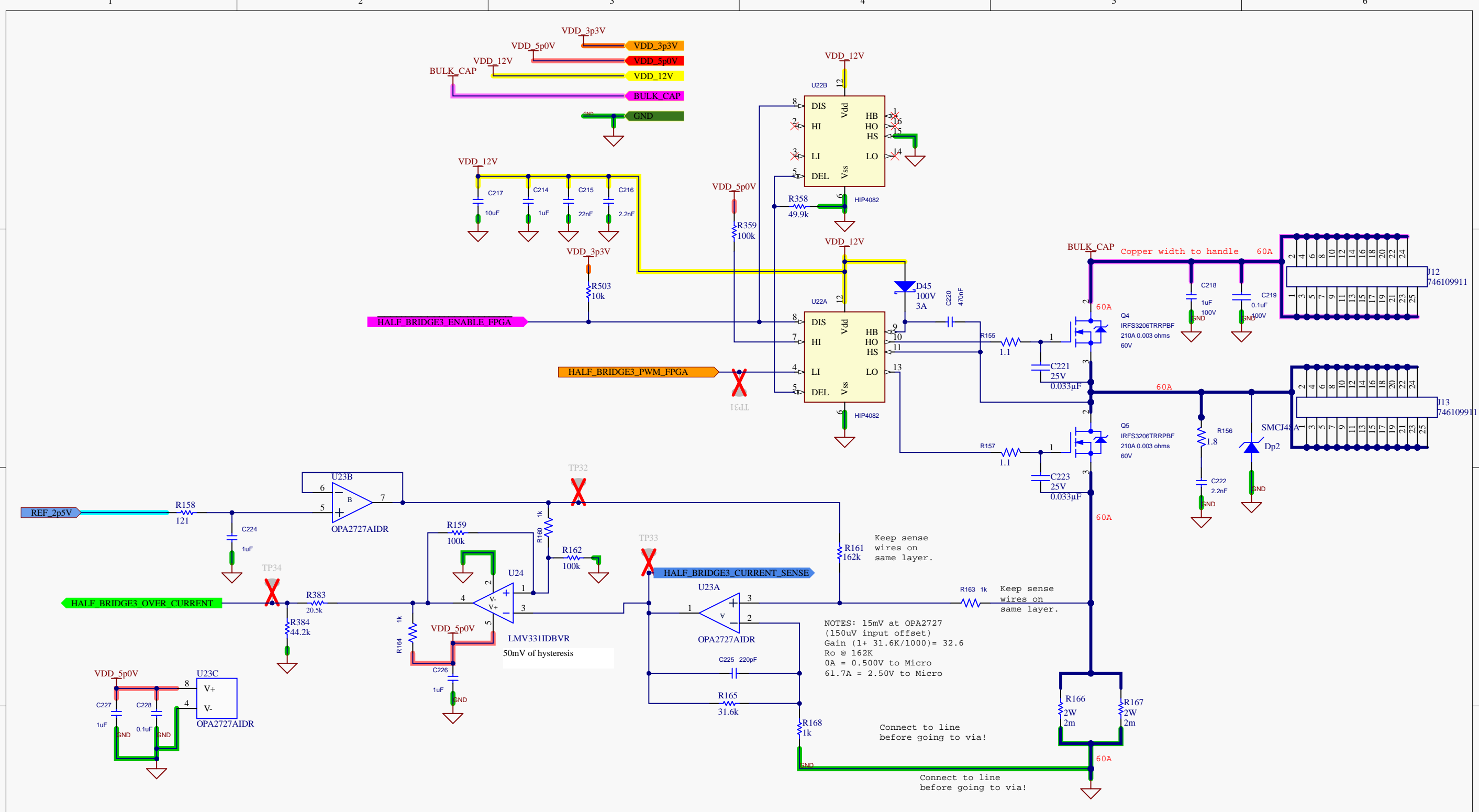
BANK 1
LCMXO3LF-2100C-5BG256I

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04 Hardware For Micro and FPGA.SchDoc
Title
SATURN SERIES TBR3206
MACHINE CONTROLLER
Document Number Q26051-002
Date: 12/18/2024
Rev E
Size: C
Engineer RDH
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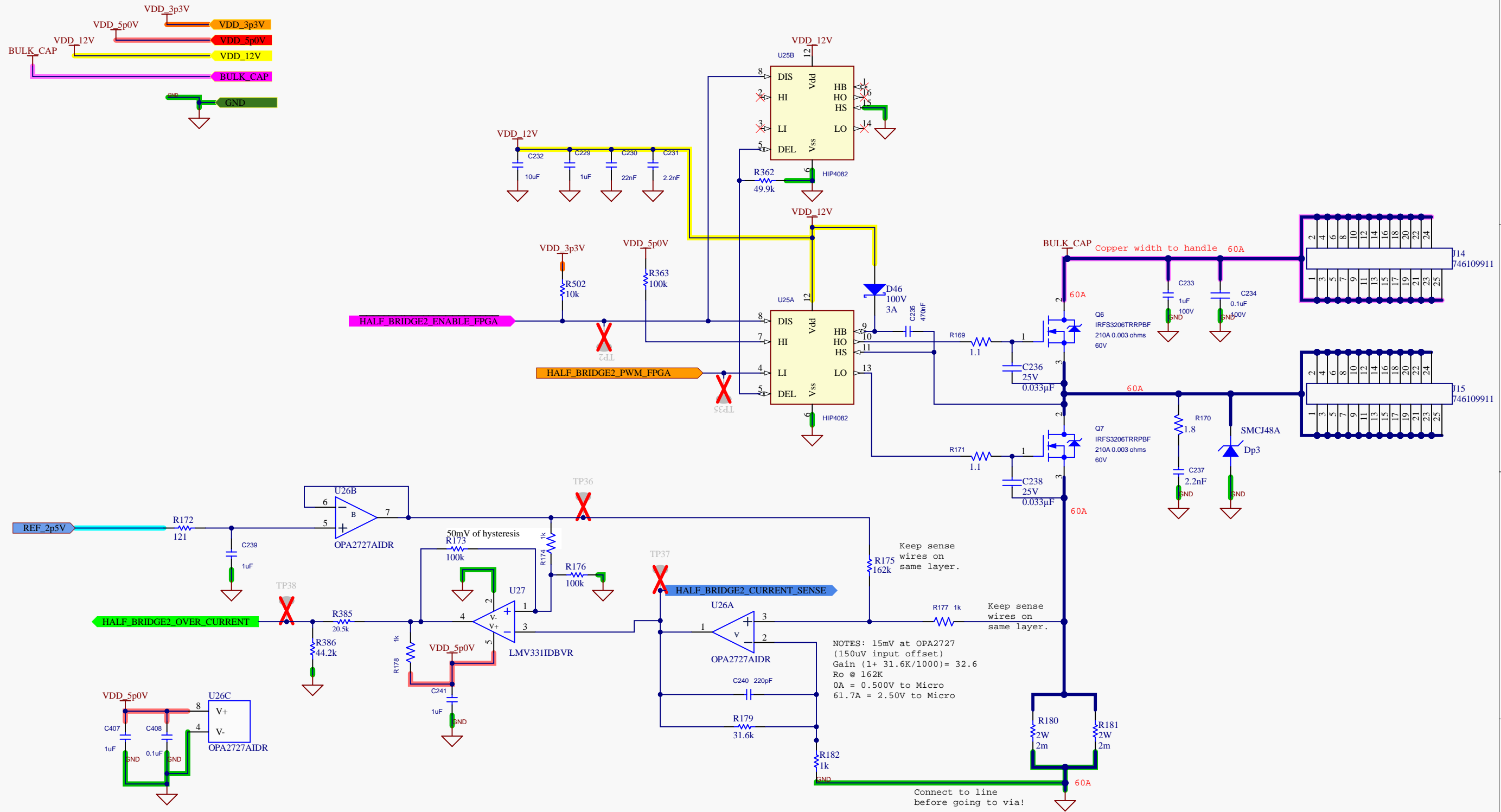


NOTES: 15mV at OPA2727
 (150uV input offset)
 Gain (1+ 31.6K/1000)= 32.6
 Ro @ 162K
 0A = 0.500V to Micro
 61.7A = 2.50V to Micro

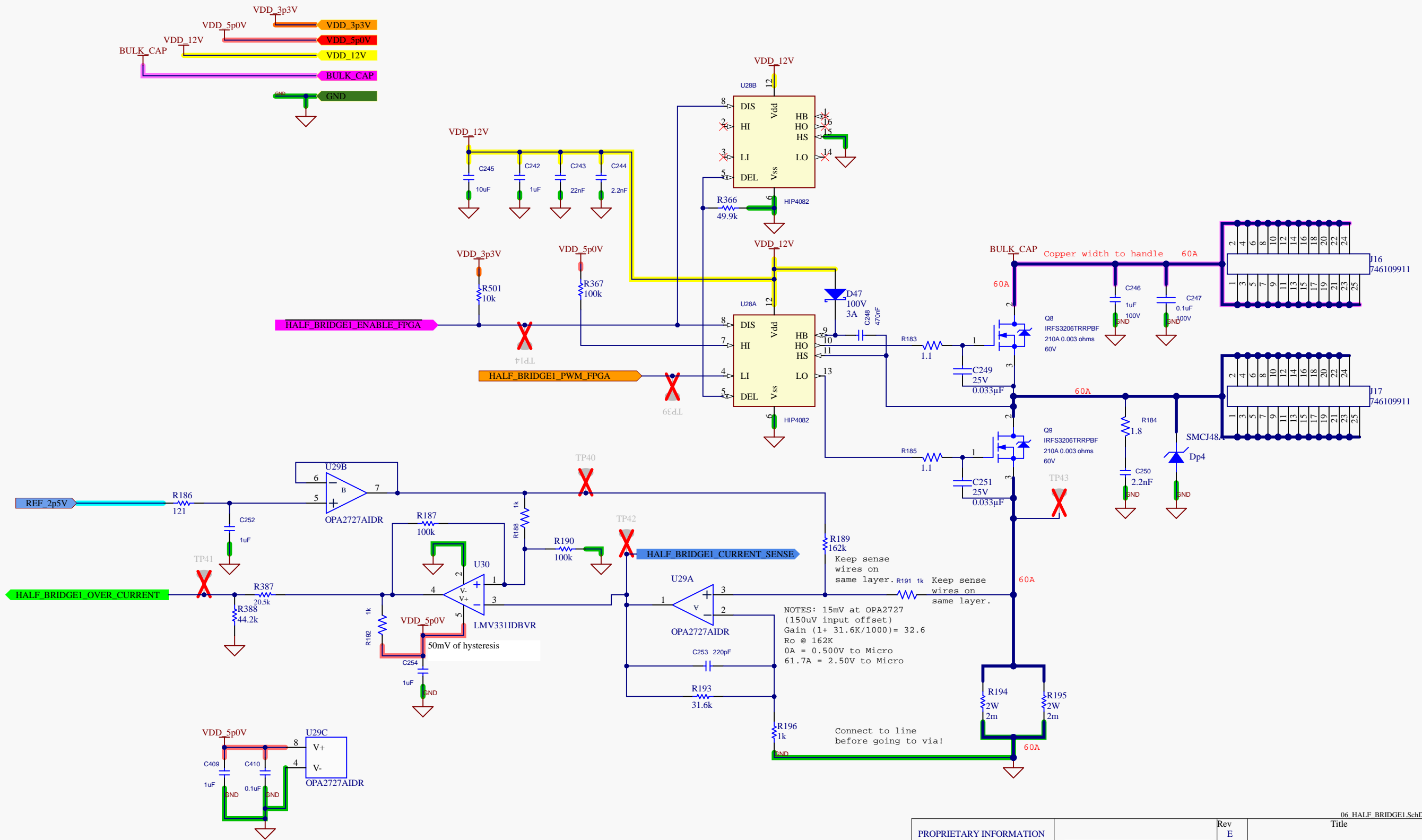
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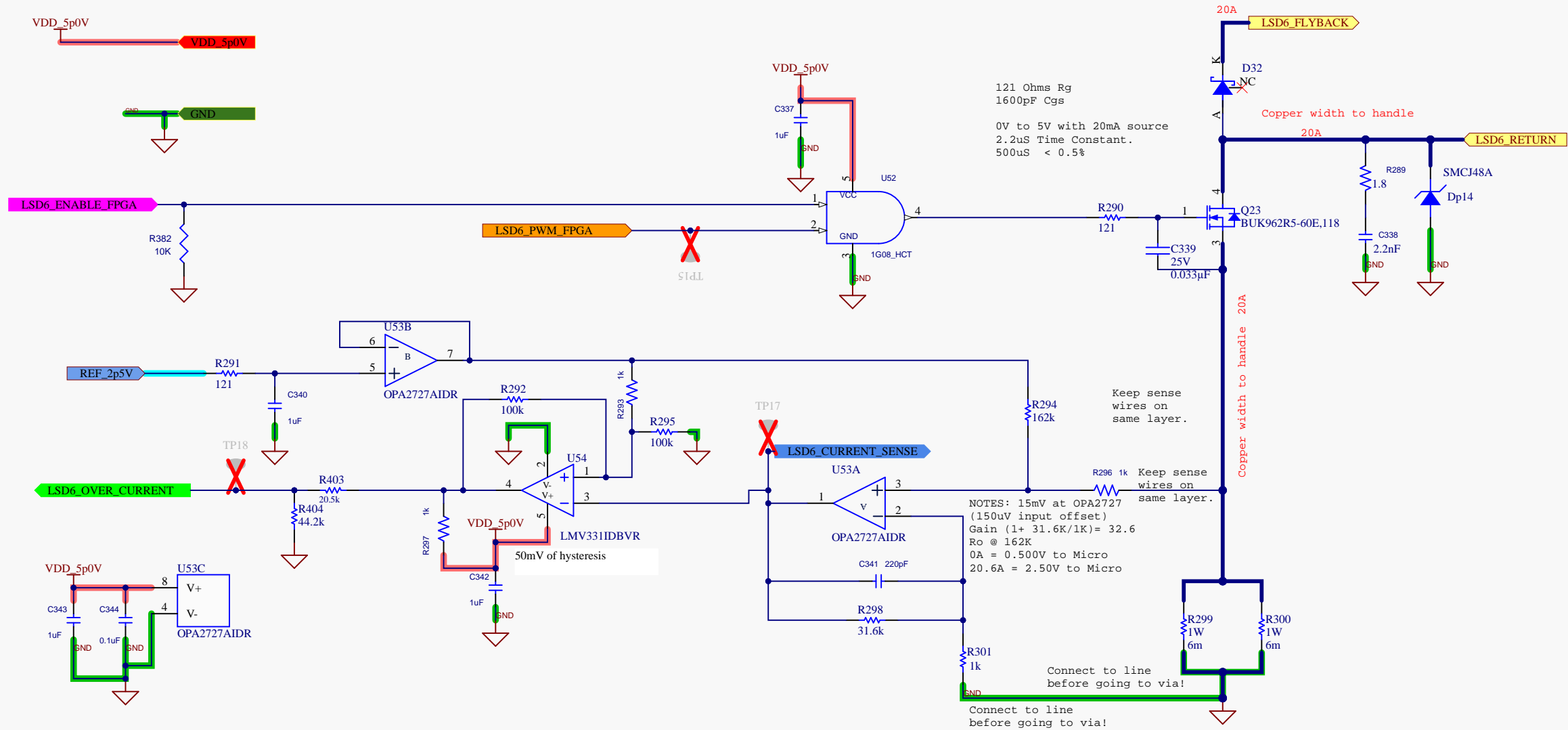
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06_HALF_BRIDGE1.SchDoc

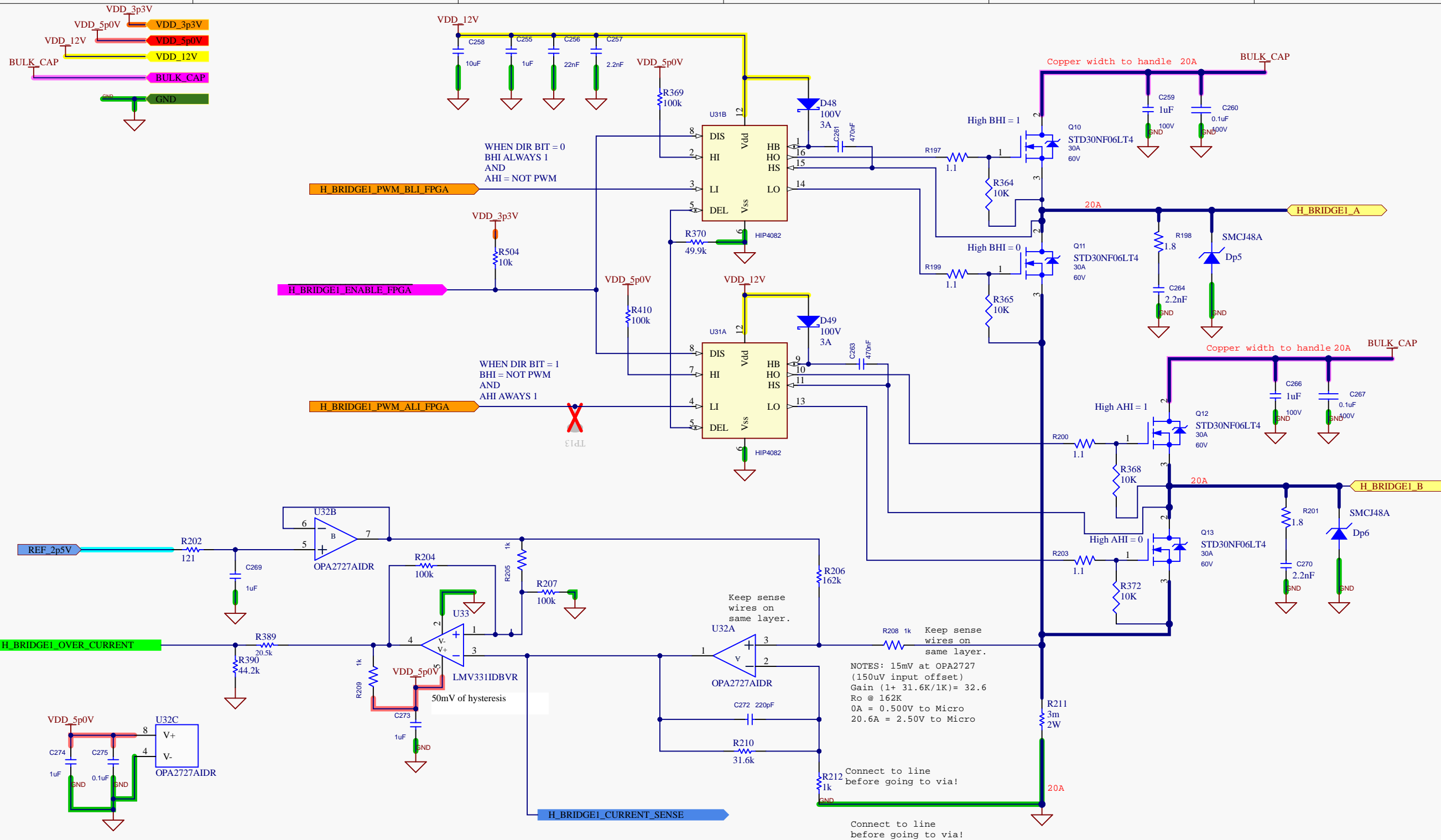
20A



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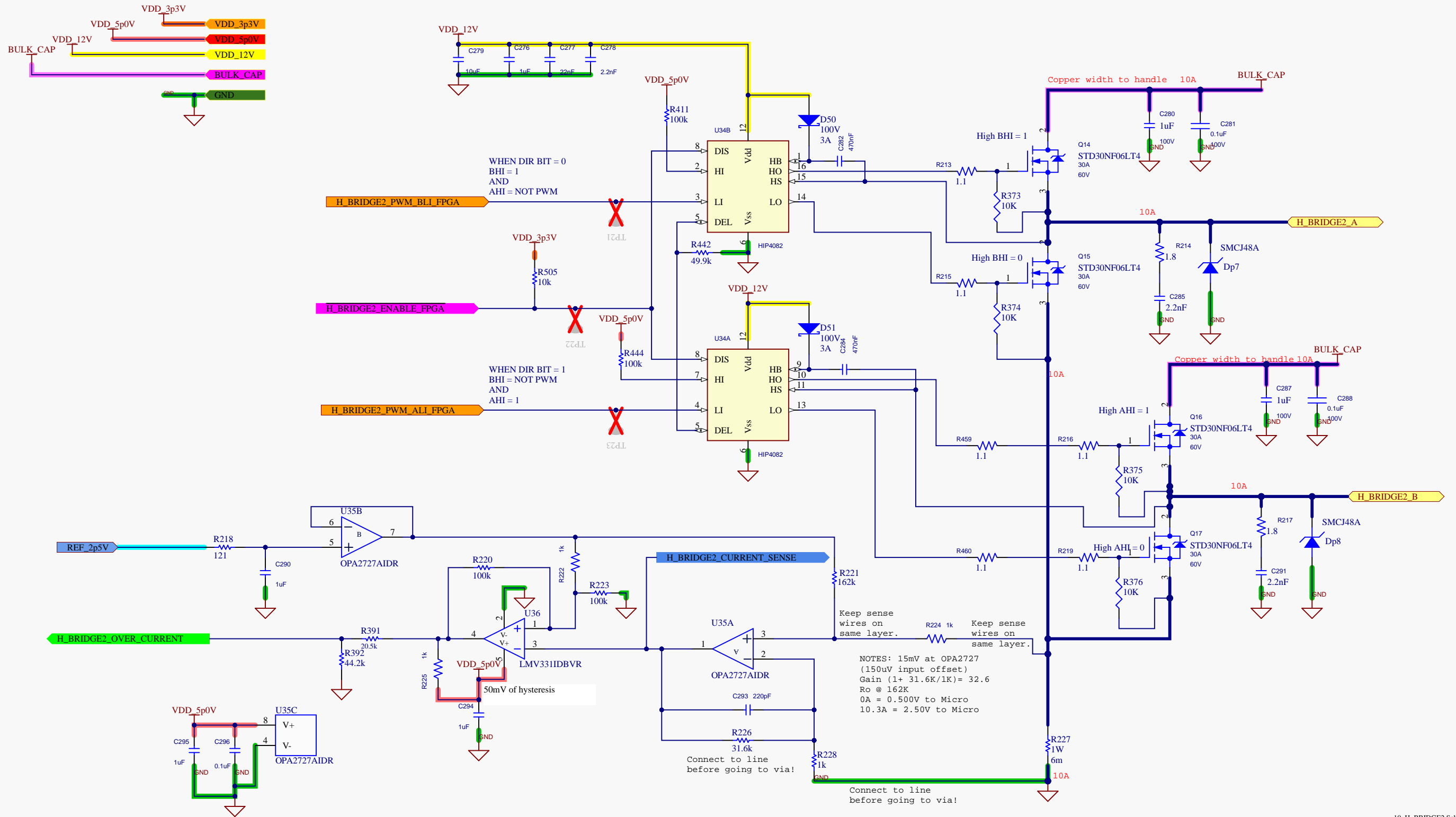


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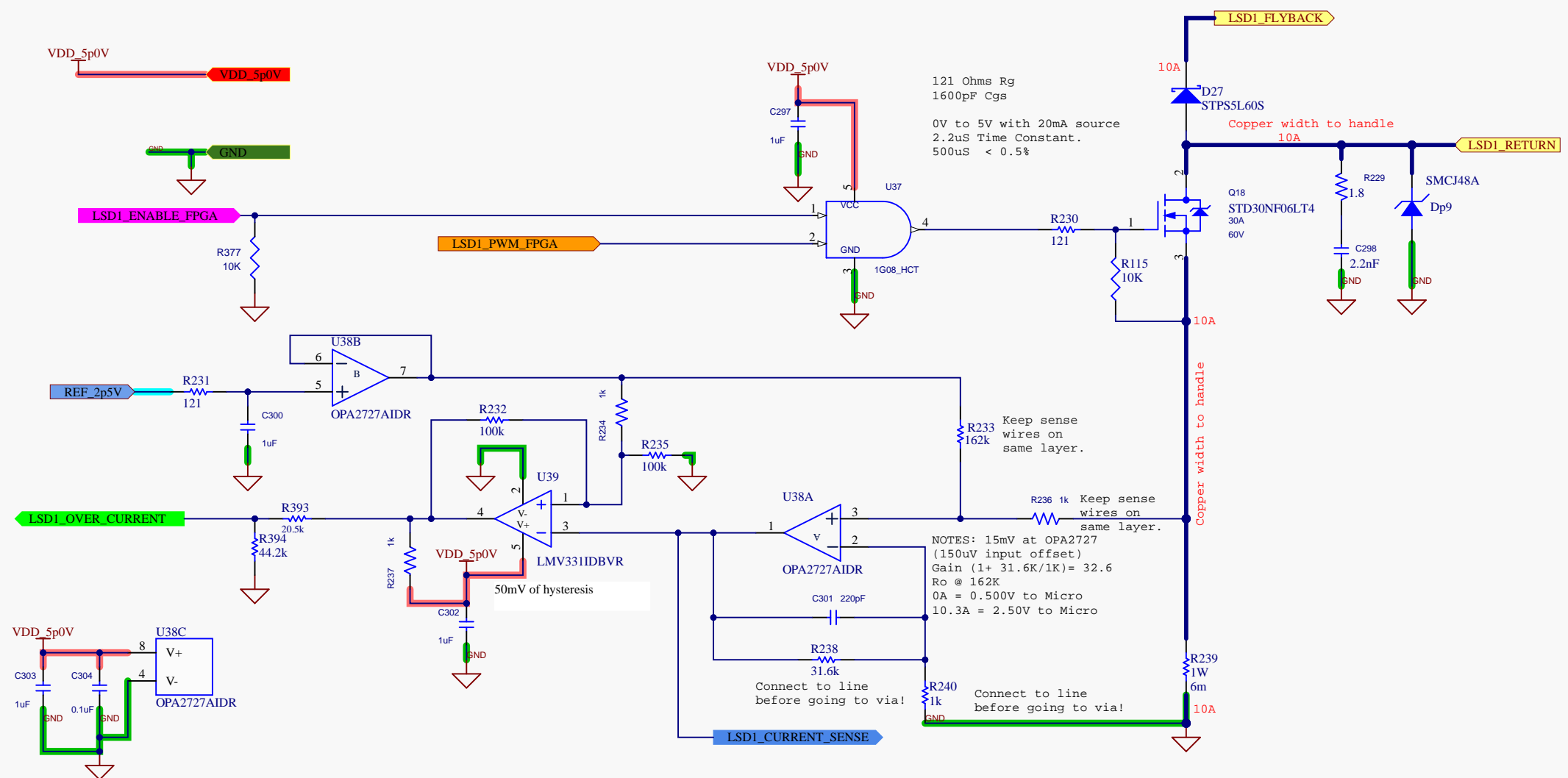
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10A



121 Ohms Rg
1600pF Cgs
0V to 5V with 20mA source
2.2uS Time Constant.
500uS < 0.5%

Keep sense wires on same layer.

Keep sense wires on same layer.

NOTES: 15mV at OPA2727 (150uV input offset)
Gain (1+ 31.6K/1K) = 32.6
Ro @ 162K
0A = 0.500V to Micro
10.3A = 2.50V to Micro

Connect to line before going to via!

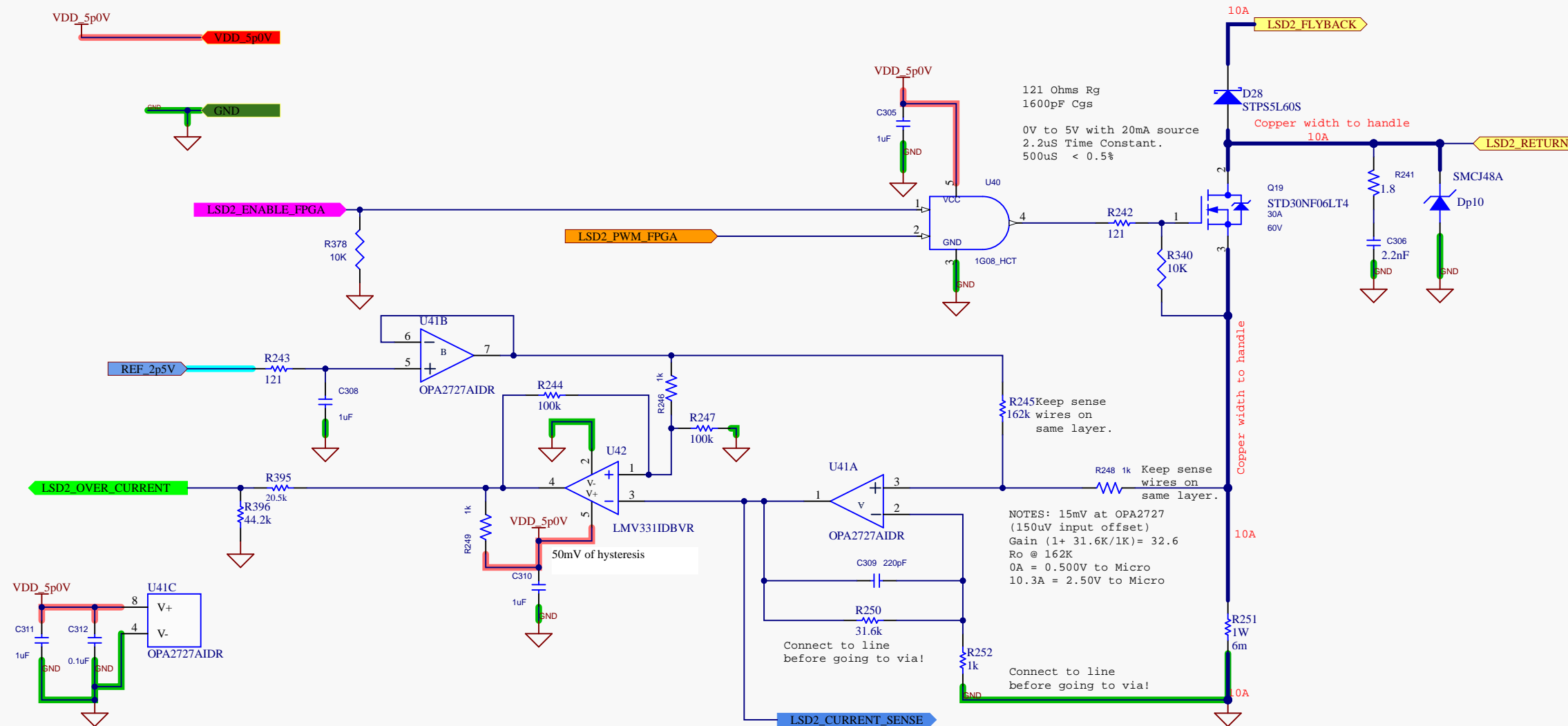
Connect to line before going to via!

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10A

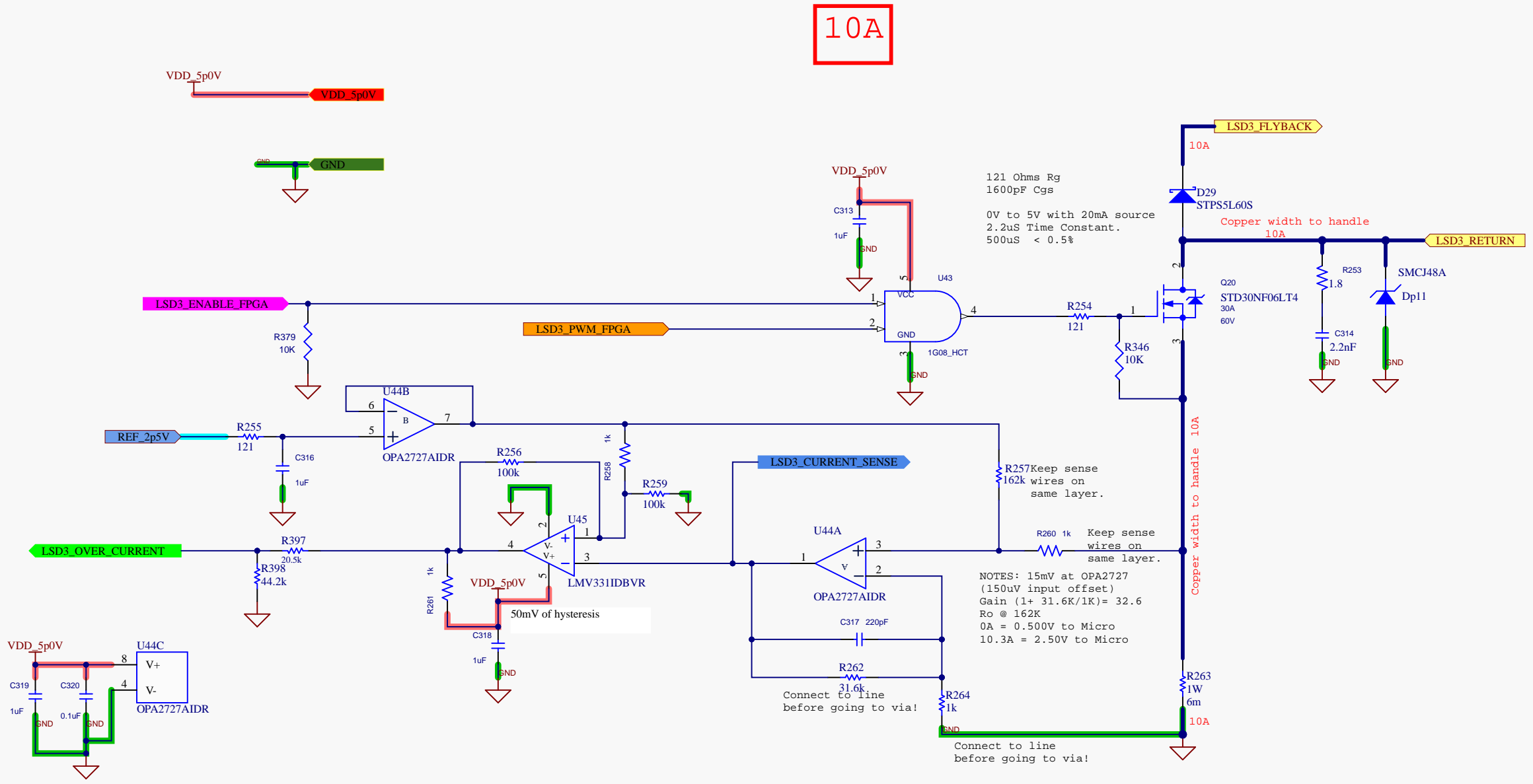


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10A

121 Ohms Rg
1600pF Cgs
0V to 5V with 20mA source
2.2uS Time Constant.
500uS < 0.5%

NOTES: 15mV at OPA2727
(150uV input offset)
Gain (1+ 31.6K/1K)= 32.6
Ro @ 162K
0A = 0.500V to Micro
10.3A = 2.50V to Micro

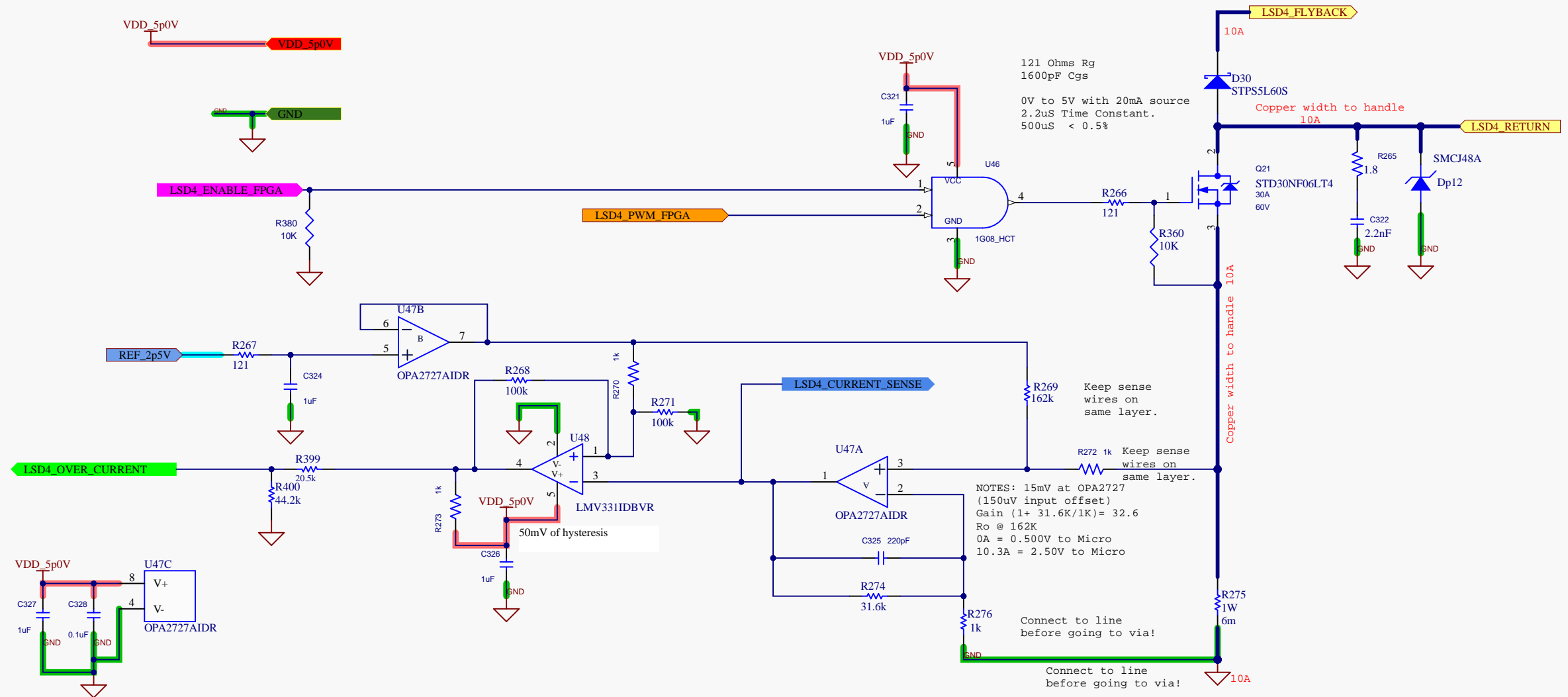
Connect to line before going to via!

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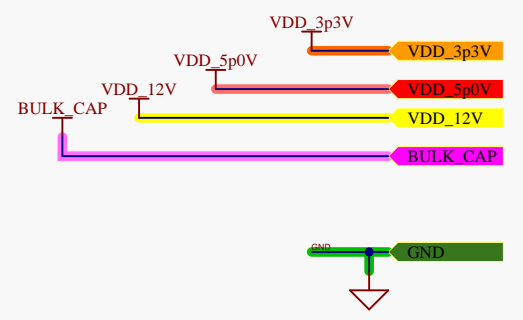


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10A

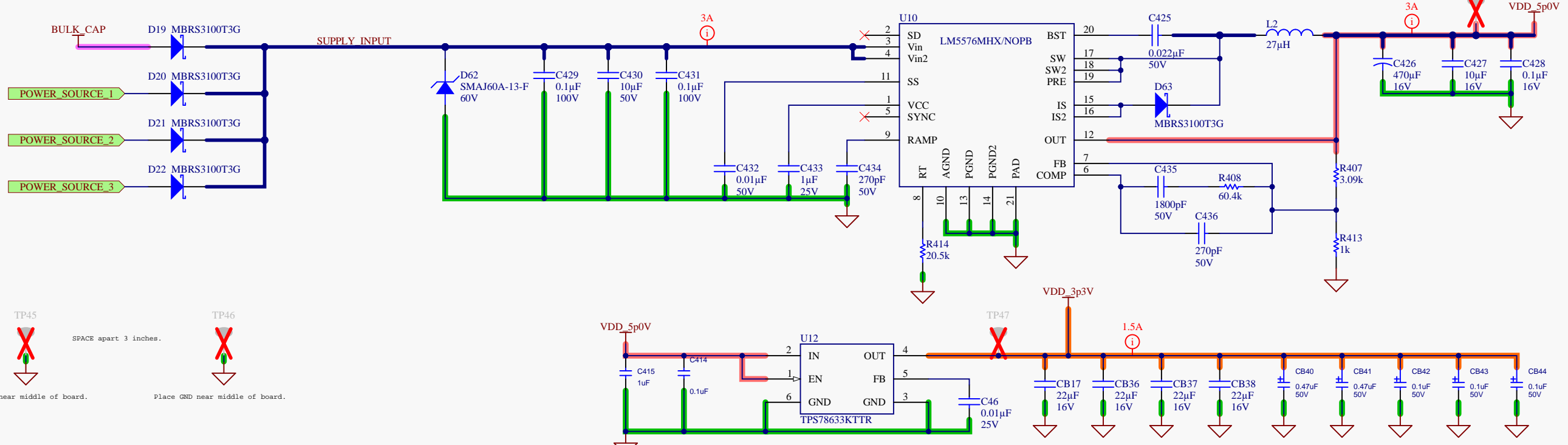


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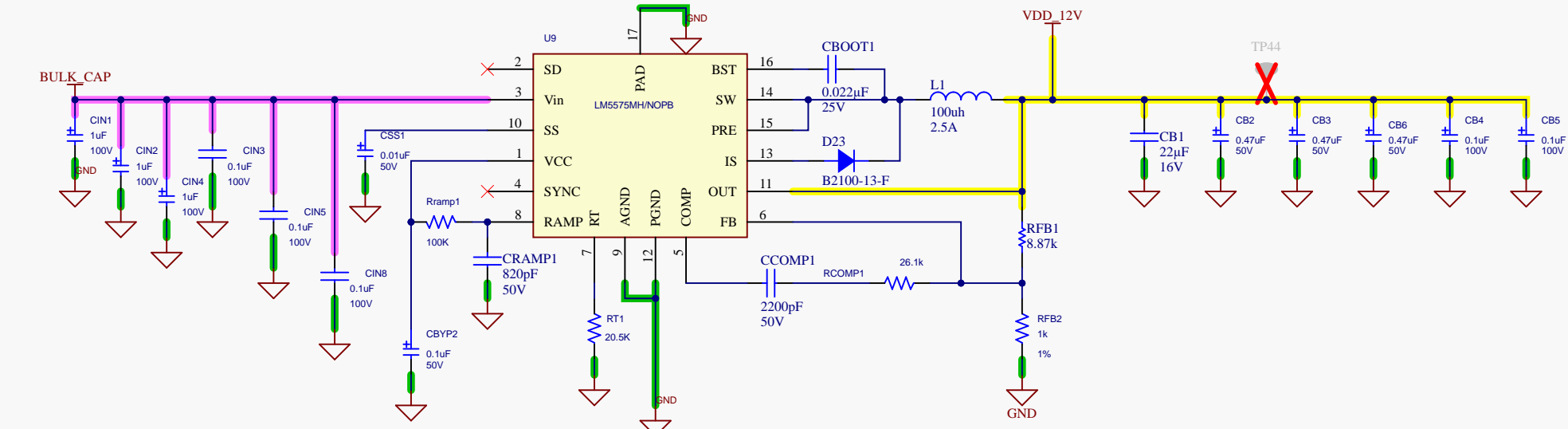


POWER INPUT
52.2V MAX.
+36V/+24/+1.2 NOMINAL
+6V MIN

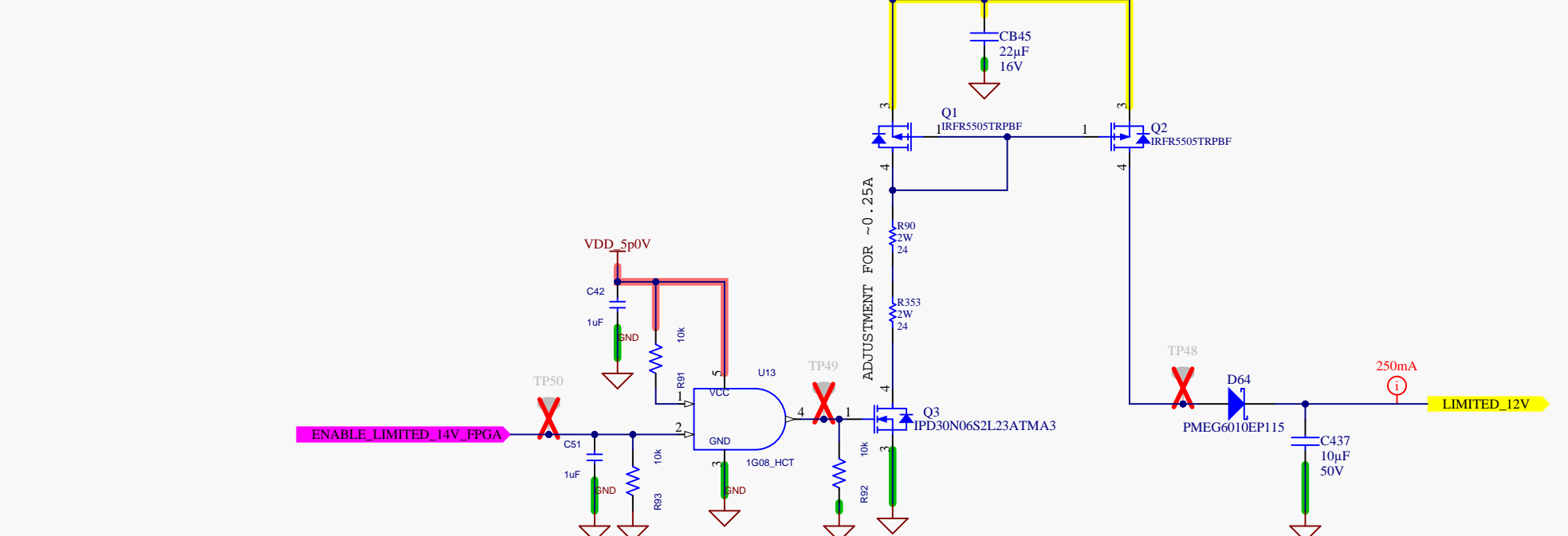
5V



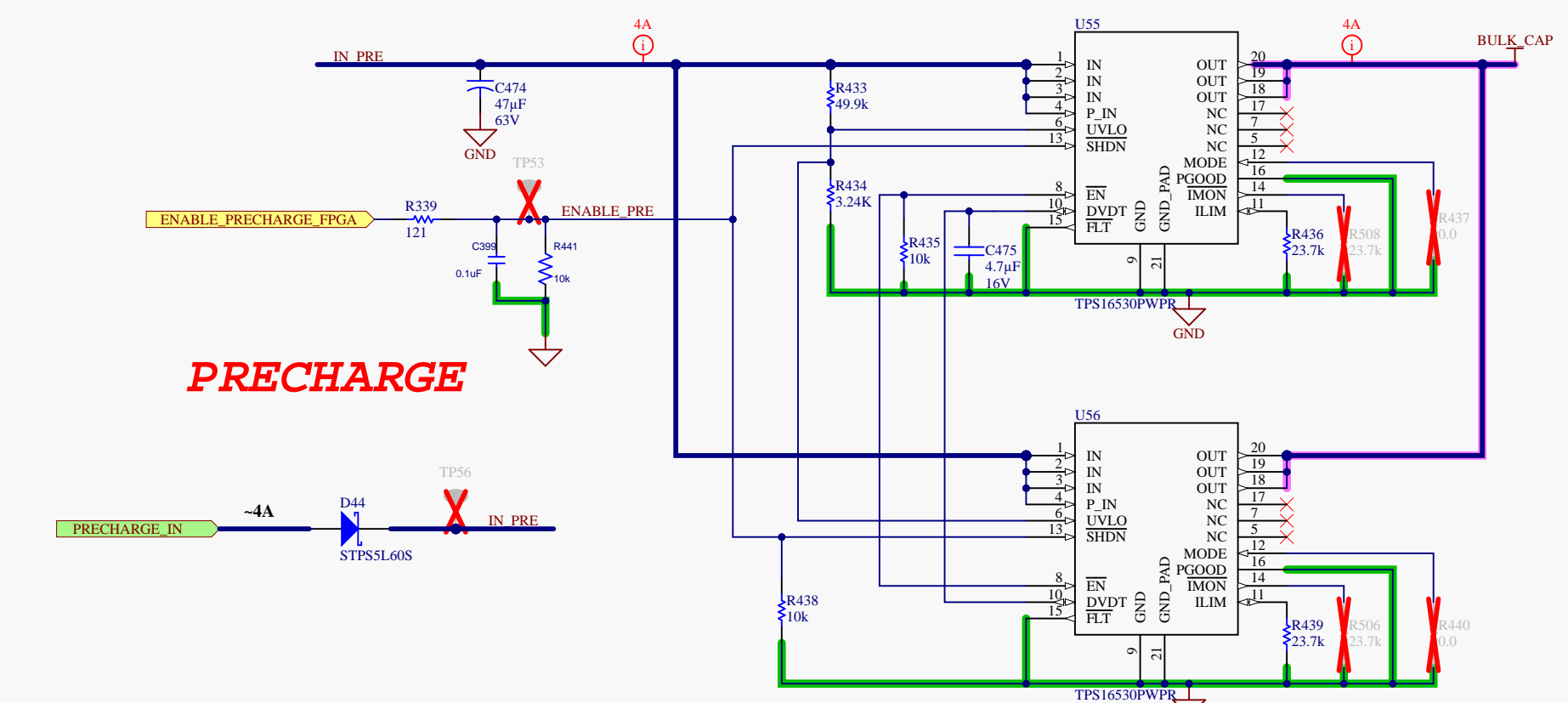
12V



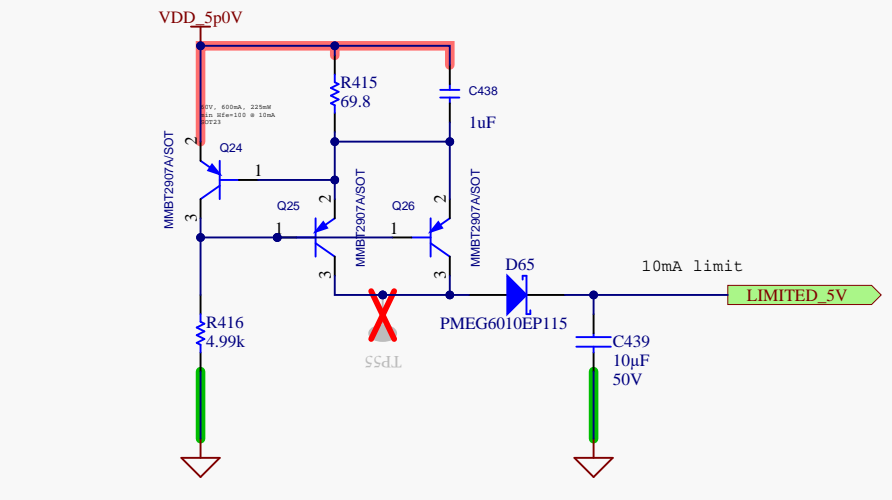
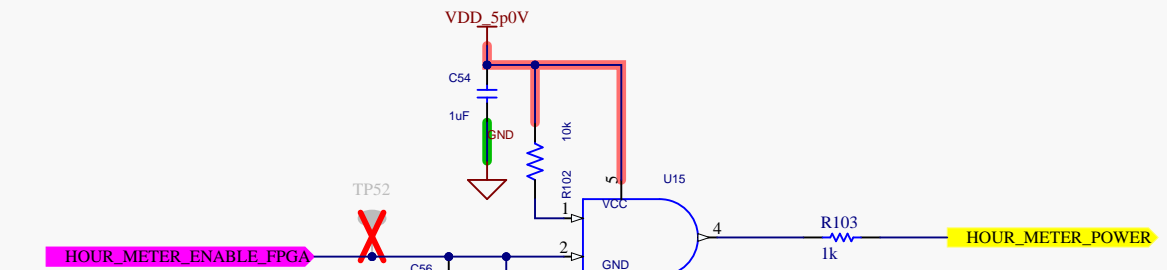
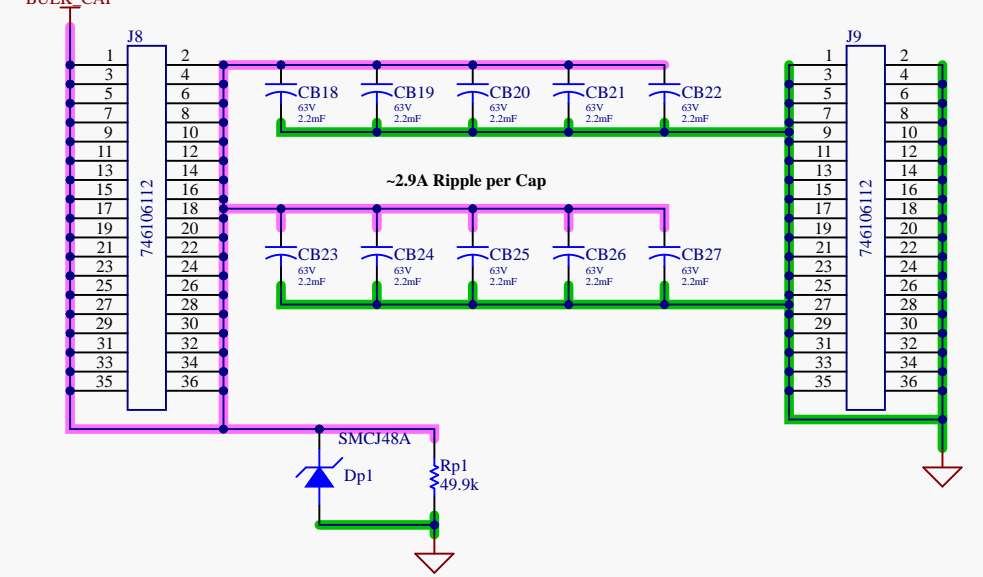
VDD_12V



PRECHARGE

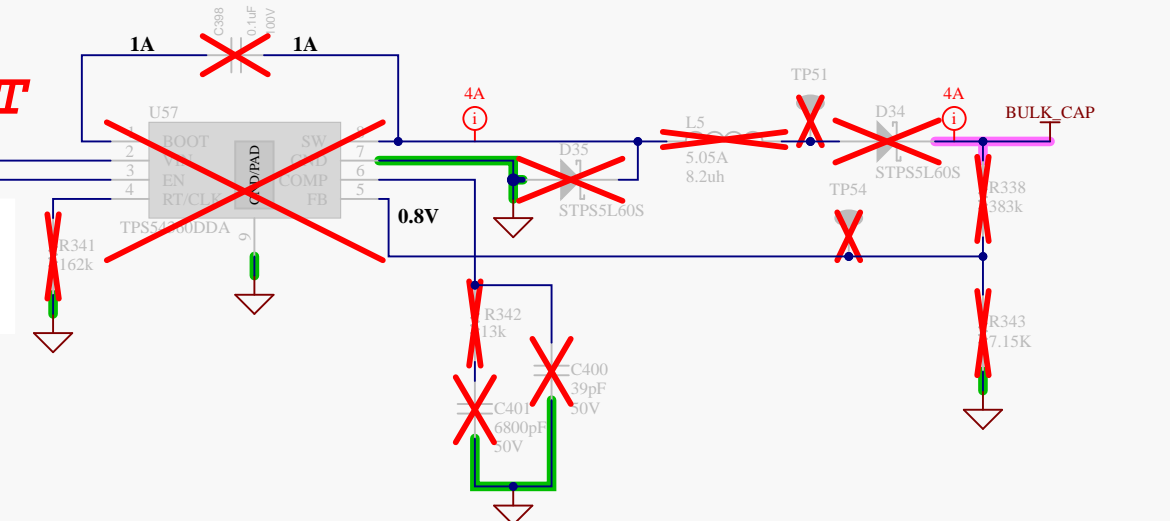


B+ ~30-36A Ripple

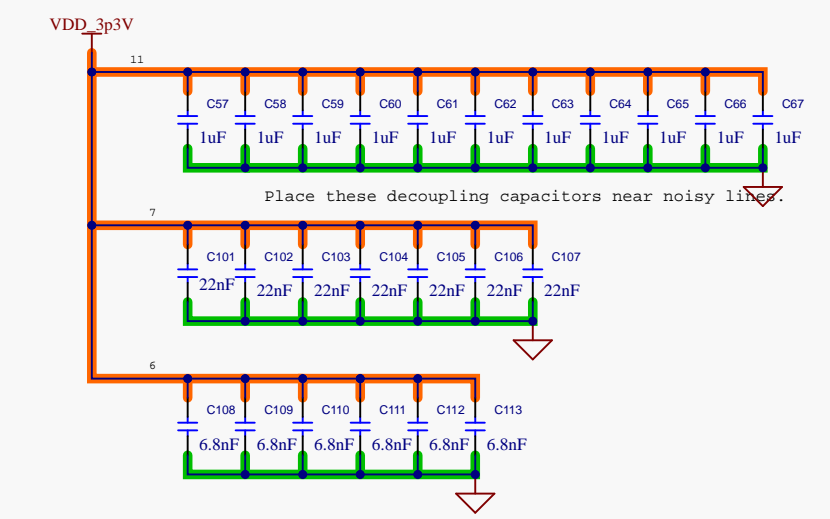
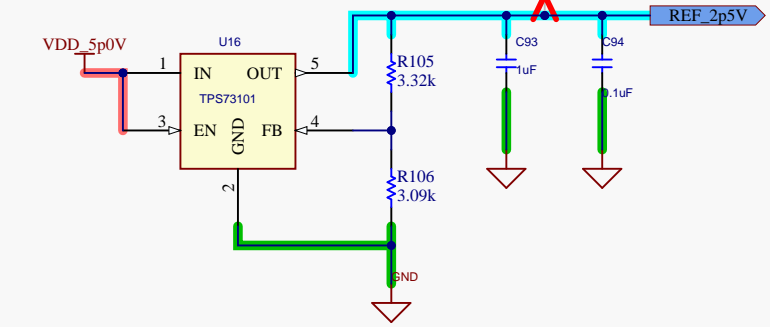


PRECHARGE ALT

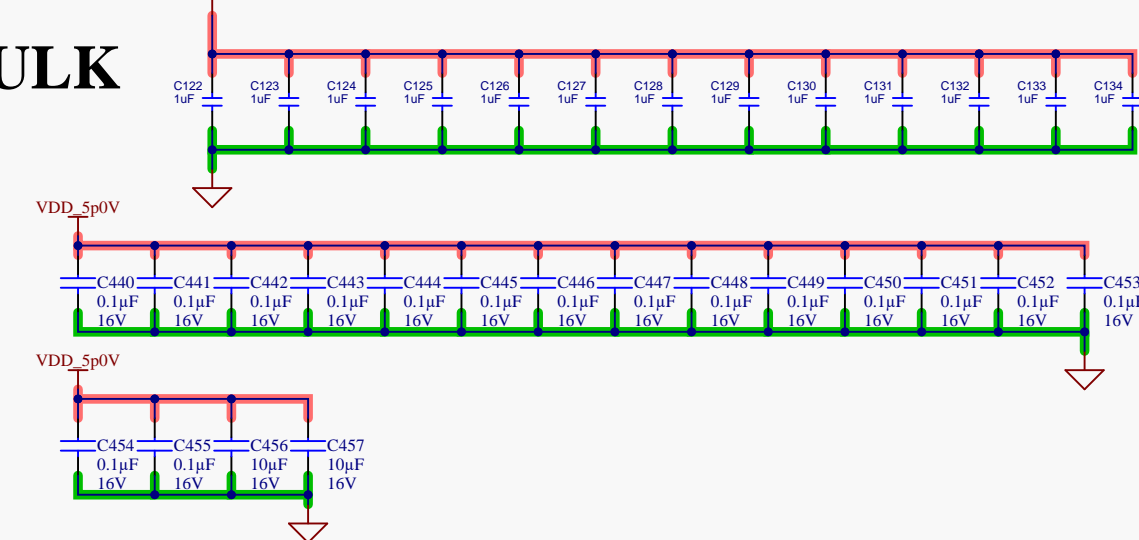
Setting Buck to 44V to charge to. Worst case scenario is 52V. When Buck gets to within 80% of VBATT or after predetermined time. Whichever comes first. Micro will then turn off Buck.



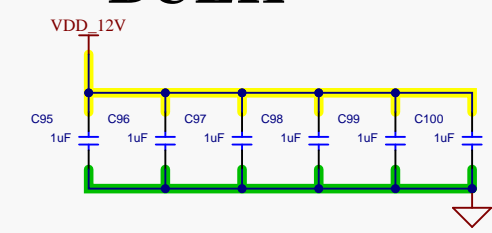
2.5V REF



BULK



BULK



3.3V

