ARM MPU AM335X Lightning Touchscreen Controller UI 15x15 Package

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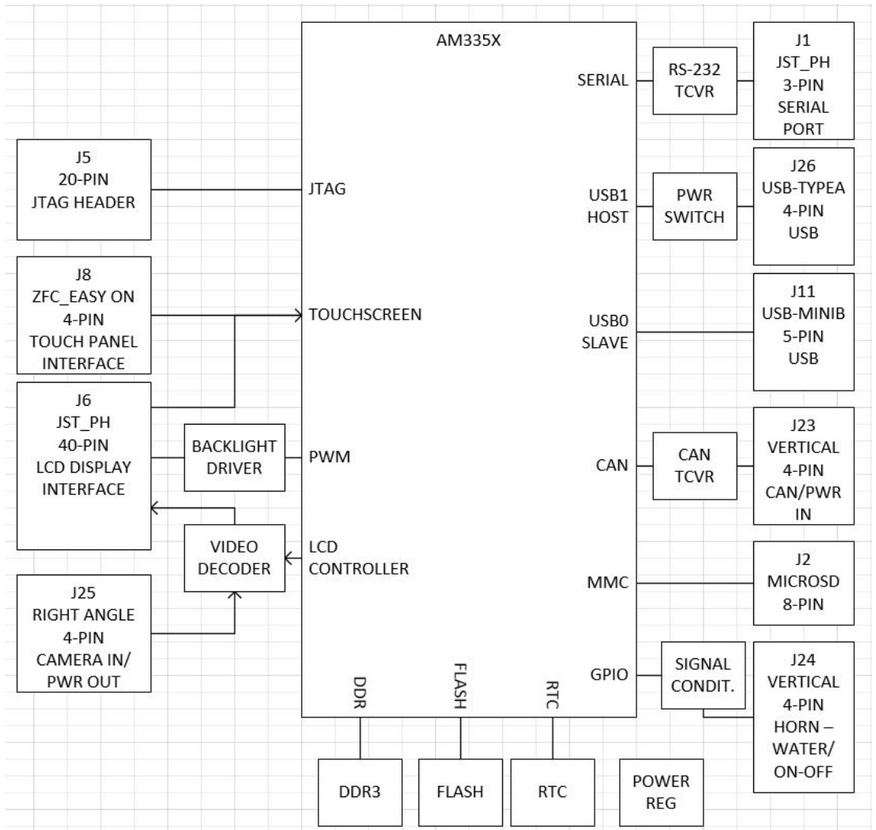

REVISIONS:
- -- Initial Release

A -- Added USB OTG Support.

B -- Added 2nd USB Port. Added USB Type A bulkhead connector. Changed USB Mini connector to a bulkhead connector.

C -- Re-annotated reference designators based on layout placement.

D - removed Jumper.

E - Adjusted Initialization Resistors from 10k to 2k

F - Changed Connector to bottom connection (4 pin lif)

(REFERENCE ONLY) PCA VARIANTS:
STANDARD 1208074

PCB1
PCB Q25061-001

SCHEMATIC1
SCHEMATIC Q26009-001

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AM335x

15mm x 15mm Package

INTERNAL RTC ELIMINATED BECAUSE WE ARE USING EXTERNAL RTC.

POPULATE R99 ONLY IF USING LARGER DDRAM IC OPTION.

IF RTC USED, RTC_PWRONRSTn NEEDS 1.8V LEVEL (VDDS_RTC) IF RTC NOT USED, CONNECT TO VSS.

LEVEL IS VDDIO IS 3.3V

NEEDS 3.3V LEVEL (VDDSHV6)

BOARD REVISION BIT DECODER:

BIT	2	1	0	
REV 0	0	0	0	P1 BOARD
REV 1	0	0	1	P1.5 BOARD
REV 2	0	1	0	P2 BOARD
REV 3	0	1	1	
REV 4	1	0	0	

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NEED TO CHECK THESE PINS TO ENSURE PROPER FUNCTIONALITY OF RTC.

WITH RTC UNUSED, PMIC_PWR_EN IS SUPPOSED TO BE N.C.

WITH RTC UNUSED, EXT_WAKEUP IS SUPPOSED TO GO TO VSS.

DGND

U12B

AM335X

15mm x 15mm Package

C6 PMIC_POWER_EN
C5 EXT_WAKEUP

8 AM335X_Xleft
8 AM335X_XRight
8 AM335X_YUp
8 AM335X_YDown

B6 AIN0
C7 AIN1
B7 AIN2
A7 AIN3
C8 AIN4
B8 AIN5
A8 AIN6
C9 AIN7

R66 10K
R65 10K

4 VDDA_ADC
4 GNDA_ADC
C60 0.1uF 16V
C59 0.001uF
VREFP_ADC

B9 VREFP
A9 VREFN

3 SPI0_SCK — A17 SPI0_SCLK [SPI0_SCLK/UART2_RXD/I2C2_SDA/EHRPWM0A/PR1_UART0_CTS_N/PR1_EDIO_SOF/EMU2/GPIO0_2]
3 SPI0_SD0 — B17 SPI0_D0 [SPI0_D0/UART2_TXD/I2C2_SCL/EHRPWM0B/PR1_UART0_RTS_N/PR1_EDIO_LATCH_IN/EMU3/GPIO0_3]
3 SPI0_SD1 — B16 SPI0_D1 [SPI0_D1/MMC1_SDWP/I2C1_SDA/EHRPWM0_TRIPZONE_INPUT/PR1_UART0_RXD/PR1_EDIO_DATA_IN0/PR1_EDIO_DATA_OUT0/GPIO0_4]
3 SPI0_CS0 — A16 SPI0_CS0 [SPI0_CS0/MMC2_SDWP/I2C1_SCL/EHRPWM0_SYNCI/PR1_UART0_TXD/PR1_EDIO_DATA_IN1/PR1_EDIO_DATA_OUT1/GPIO0_5]
7 SD_CARD_DETECT — C15 SPI0_CS1 [SPI0_CS1/UART3_RXD/ECAP1_IN_PWM1_OUT/HMC0_POW/XDMA_EVENT_INTR2/MMC0_SDCD/EMU4/GPIO0_6]

6 AM335X_UART0_TXD — E16 UART0_TXD [UART0_TXD/SPI1_CS1/DCAN0_RX/I2C2_SCL/ECAP1_IN_PWM1_OUT/PR1_PRU1_PRU_R30_15/PR1_PRU1_PRU_R31_15/GPIO1_11]
6 AM335X_UART0_RXD — E15 UART0_RXD [UART0_RXD/SPI1_CS0/DCAN0_TX/I2C2_SDA/ECAP2_IN_PWM2_OUT/PR1_PRU1_PRU_R30_14/PR1_PRU1_PRU_R31_14/GPIO1_10]
E18 UART0_CTSn [UART0_CTSN/UART4_RXD/DCAN1_TX/I2C1_SDA/SPI1_D0/TIMER7/PR1_EDC_SYNC0_OUT/GPIO1_8]
E17 UART0_RTSn [UART0_RTSN/UART4_TXD/DCAN1_RX/I2C1_SCL/SPI1_D1/SPI1_CS0/PR1_EDC_SYNC1_OUT/GPIO1_9]

VDDSHV6

8 LCD_BACKLIGHT_HI — D15 UART1_TXD [UART1_TXD/MMC2_SDWP/DCAN1_RX/I2C1_SCL//PR1_UART0_TXD/PR1_PRU0_PRU_R31_16/GPIO0_15]
D16 UART1_RXD [UART1_RXD/MMC1_SDWP/DCAN1_TX/I2C1_SDA//PR1_UART0_RXD/PR1_PRU1_PRU_R31_16/GPIO0_14]
D18 UART1_CTSn [UART1_CTSN/TIMER6/DCAN0_TX/I2C2_SDA/SPI1_CS0/PR1_UART0_CTS_N/PR1_EDC_LATCH0_IN/GPIO0_12]
6 CAN0_TX — D17 UART1_RTSn [UART1_RTSN/TIMER5/DCAN0_RX/I2C2_SCL/SPI1_CS1/PR1_UART0_RTS_N/PR1_EDC_LATCH1_IN/GPIO0_13]
6 CAN0_RX

R57 4.75K
R56 4.75K

5,7,9 AM335X_I2C0_SCL — C16 I2C0_SCL [I2C0_SCL/TIMER7/UART2_RTSN/ECAP1_IN_PWM1_OUT////GPIO3_6]
5,7,9 AM335X_I2C0_SDA — C17 I2C0_SDA [I2C0_SDA/TIMER4/UART2_CTSN/ECAP2_IN_PWM2_OUT////GPIO3_5]

6 USB0_DP — N17 USB0_DP
6 USB0_DM — N18 USB0_DM
USB0 ACTIVE HIGH CHARGER ENABLE OUTPUT — M15 USB0_CE
P16 USB0_ID
F16 USB0_DRVVBUS [USB0_DRVVBUS//////GPIO0_18]
P15 USB0_VBUS

USB_VBUS PINS ARE THE ONLY ONES THAT ARE 5V TOLERANT.

6 VUSB_VBUS

6 USB1_DP — R17 USB1_DP
6 USB1_DM — R18 USB1_DM
USB1 ID should be tied to GND for host operation. — P18 USB1_CE
USB1_ID — P17 USB1_ID
6 USB1_DRVVBUS — T15 USB1_DRVVBUS [USB1_DRVVBUS//////GPIO3_13]
6 VUSB_VBUS1 — T18 USB1_VBUS

R137 0

C18 ECAP0_IN_PWM0_OUT [ECAP0_IN_PWM0_OUT/UART3_TXD/SPI1_CS1/PR1_ECAP0_ECAP_CAPIN_APWM_O/SPI1_SCLK/MMC0_SDWP/XDMA_EVENT_INTR2/GPIO0_7]

AM335X_15x15

DGND

If USB0 or USB1 is not used...
--Connect the respective VDDA1P8V_USB terminal to any 1.8-V power supply and respective VDDA3P3V_USB terminal to any 3.3-V power supply. If the system does not have a 3.3-V power supply, the VDDA3P3V_USB terminal may be connected to ground.
--The OTG_PWRDN and CM_PWRDN bits in the respective USB_CTRL register can be used to power down the unused USB PHY to minimize power supply leakage current. These bits default to the powered-up state after the AM335x device has been reset. The USB PHY can be powered down by setting both of these bits to "1".
--The respective VBUS, ID, DP, and DM terminals may be connected to ground or left floating.
--The respective CE terminal should be left floating.

(USB_ID) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSSA_USB with a resistance less than 10 O or greater than 100 kO. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.

[GMII1_TXCLK/UART2_RXD/RGMII1_TCLK/MMC0_DAT7//MMC1_DAT0/UART1_DCDN/MCASP0_ACLKX/GPIO3_9] MII1_TXCLK — K18
[GMII1_TXD0/RMII1_TXD0/RGMII1_TD0/MCASP1_AXR2/MCASP1_ACLKR/EQEP0B_IN/MMC1_CLK/GPIO0_28] MII1_TXD0 — K17
[GMII1_TXD1/RMII1_TXD1/RGMII1_TD1/MCASP1_FSR/MCASP1_AXR1/EQEP0A_IN/MMC1_CMD/GPIO0_21] MII1_TXD1 — K16
[GMII1_TXD2/DCAN0_RX/RGMII1_TD2/UART4_TXD/MCASP1_AXR0/MMC2_DAT2/MCASP0_AHCLKX/GPIO0_17] MII1_TXD2 — K15
[GMII1_TXD3/DCAN0_TX/RGMII1_TD3/UART4_RXD/MCASP1_FSX/MMC2_DAT1/MCASP0_FSR/GPIO0_16] MII1_TXD3 — J18
[GMII1_TXEN/RMII1_TXEN/RGMII1_TCTL/TIMER4/MCASP1_AXR0/EQEP0_INDEX/MMC2_CMD/GPIO3_3] MII1_TXEN — J16
[GMII1_CRS/RMII1_CRS_DV/SPI1_D0/I2C1_SDA/MCASP1_ACLKX/UART5_CTSN/UART2_RXD/GPIO3_1] MII1_CRS — H17
[GMII1_COL/RMII2_REFCLK/SPI1_SCLK/UART5_RXD/MCASP1_AXR2/MMC2_DAT3/MCASP0_AXR2/GPIO3_0] MII1_COL — H16

GPIO3_9 — AM335x_WTR_SW 6
GPIO0_16 — AM335x_HORN_SW6

[GMII1_RXCLK/UART2_TXD/RGMII1_RCLK/MMC0_DAT6/MMC1_DAT1/UART1_DSRN/MCASP0_FSX/GPIO3_10] MII1_RXCLK — L18
[GMII1_RXD0/RMII1_RXD0/RGMII1_RD0/MCASP1_AHCLKX/MCASP1_AHCLKR/MCASP1_ACLKR/MCASP0_AXR3/GPIO2_21] MII1_RXD0 — M16
[GMII1_RXD1/RMII1_RXD1/RGMII1_RD1/MCASP1_AXR3/MCASP1_FSR/EQEP0_STROBE/MMC2_CLK/GPIO2_20] MII1_RXD1 — L15
[GMII1_RXD2/UART3_TXD/RGMII1_RD2/MMC0_DAT4/MMC1_DAT3/UART1_RIN/MCASP0_AXR1/GPIO2_19] MII1_RXD2 — L16
[GMII1_RXD3/UART3_RXD/RGMII1_RD3/MMC0_DAT5/MMC1_DAT2/UART1_DTRN/MCASP0_AXR0/GPIO2_18] MII1_RXD3 — L17
[GMII1_RXER/RMII1_RXERR/SPI1_D1/I2C1_SCL/MCASP1_FSX/UART5_RTSN/UART2_TXD/GPIO3_2] MII1_RXERR — J15
[GMII1_RXDV/LCD_MEMORY_CLK/RGMII1_RCTL/UART5_TXD/MCASP1_ACLKX/MMC2_DAT0/MCASP0_ACLKR/GPIO3_4] MII1_RXDV — J17

GPIO3_10 — DEC_RESET 9

[RMII1_REFCLK/XDMA_EVENT_INTR2/SPI1_CS0/UART5_TXD/MCASP1_AXR3/MMC0_POW/MCASP1_AHCLKX/GPIO0_29] MII1_REFCLK — H18
[MDIO_CLK/TIMER5/UART5_TXD/UART3_RTSN/MMC0_SDWP/MMC1_CLK/MMC2_CLK/GPIO0_3] MDIO_CLK — M18
[MDIO_DATA/TIMER6/UART5_RXD/UART3_CTSN/MMC0_SDCD/MMC1_CMD/MMC2_CMD/GPIO0_0] MDIO_DATA — M17

AM335X_LCD_DATA[15..0] — AM335X_LCD_DATA[15..0] 8,9

[LCD_DATA0/GPMC_A0/PR1_MII_MT0_CLK/EHRPWM2A//PR1_PRU1_PRU_R30_0/PR1_PRU1_PRU_R31_0/GPIO2_6] LCD_DATA0 — R1 — AM335X_LCD_DATA0
[LCD_DATA1/GPMC_A1/PR1_MII0_TXEN/EHRPWM2B//PR1_PRU1_PRU_R30_1/PR1_PRU1_PRU_R31_1/GPIO2_7] LCD_DATA1 — R2 — AM335X_LCD_DATA1
[LCD_DATA2/GPMC_A2/PR1_MII0_TXD3/EHRPWM2_TRIPZONE_INPUT//PR1_PRU1_PRU_R30_2/PR1_PRU1_PRU_R31_2/GPIO2_8] LCD_DATA2 — R3 — AM335X_LCD_DATA2
[LCD_DATA3/GPMC_A3/PR1_MII0_TXD2/EHRPWM2_SYNCI_O//PR1_PRU1_PRU_R30_3/PR1_PRU1_PRU_R31_3/GPIO2_9] LCD_DATA3 — R4 — AM335X_LCD_DATA3
[LCD_DATA4/GPMC_A4/PR1_MII0_TXD1/EQEP2A_IN//PR1_PRU1_PRU_R30_4/PR1_PRU1_PRU_R31_4/GPIO2_10] LCD_DATA4 — T1 — AM335X_LCD_DATA4
[LCD_DATA5/GPMC_A5/PR1_MII0_TXD0/EQEP2B_IN//PR1_PRU1_PRU_R30_5/PR1_PRU1_PRU_R31_5/GPIO2_11] LCD_DATA5 — T2 — AM335X_LCD_DATA5
[LCD_DATA6/GPMC_A6/PR1_EDIO_DATA_IN6/EQEP2_INDEX/PR1_EDIO_DATA_OUT6/PR1_PRU1_PRU_R30_6/PR1_PRU1_PRU_R31_6/GPIO2_12] LCD_DATA6 — T3 — AM335X_LCD_DATA6
[LCD_DATA7/GPMC_A7/PR1_EDIO_DATA_IN7/EQEP2_STROBE/PR1_EDIO_DATA_OUT7/PR1_PRU1_PRU_R30_7/PR1_PRU1_PRU_R31_7/GPIO2_13] LCD_DATA7 — T4 — AM335X_LCD_DATA7
[LCD_DATA8/GPMC_A12/EHRPWM1_TRIPZONE_INPUT/MCASP0_ACLKX/UART5_TXD/PR1_MII0_RXD3/UART2_CTSN/GPIO2_14] LCD_DATA8 — U1 — AM335X_LCD_DATA8
[LCD_DATA9/GPMC_A13/EHRPWM1_SYNCO/MCASP0_FSX/UART5_RXD/PR1_MII0_RXD2/UART2_RTSN/GPIO2_15] LCD_DATA9 — U2 — AM335X_LCD_DATA9
[LCD_DATA10/GPMC_A14/EHRPWM1A/MCASP0_AXR0//PR1_MII0_RXD1/UART3_CTSN/GPIO2_16] LCD_DATA10 — U3 — AM335X_LCD_DATA10
[LCD_DATA11/GPMC_A15/EHRPWM1B/MCASP0_AHCLKR/MCASP0_AXR2/PR1_MII0_RXD0/UART3_RTSN/GPIO2_17] LCD_DATA11 — U4 — AM335X_LCD_DATA11
[LCD_DATA12/GPMC_A16/EQEP1A_IN/MCASP0_ACLKR/MCASP0_AXR2/PR1_MII0_RXLINK/UART4_CTSN/GPIO0_8] LCD_DATA12 — V2 — AM335X_LCD_DATA12
[LCD_DATA13/GPMC_A17/EQEP1B_IN/MCASP0_FSR/MCASP0_AXR3/PR1_MII0_RXER/UART4_RTSN/GPIO0_9] LCD_DATA13 — V3 — AM335X_LCD_DATA13
[LCD_DATA14/GPMC_A18/EQEP1_INDEX/MCASP0_AXR1/UART5_RXD/PR1_MII_MR0_CLK/UART5_CTSN/GPIO0_10] LCD_DATA14 — V4 — AM335X_LCD_DATA14
[LCD_DATA15/GPMC_A19/EQEP1_STROBE/MCASP0_AHCLKX/MCASP0_AXR3/PR1_MII0_RXDV/UART5_RTSN/GPIO0_11] LCD_DATA15 — T5 — AM335X_LCD_DATA15

[LCD_PCLK/GPMC_A10/PR1_MII0_CRS/PR1_EDIO_DATA_IN4/PR1_EDIO_DATA_OUT4/PR1_PRU1_PRU_R30_10/PR1_PRU1_PRU_R31_10/GPIO2_24] LCD_PCLK — V5 — AM335X_LCD_PCLK 9
[LCD_VSYNC/GPMC_A8//PR1_EDIO_DATA_IN2/PR1_EDIO_DATA_OUT2/PR1_PRU1_PRU_R30_8/PR1_PRU1_PRU_R31_8/GPIO2_22] LCD_VSYNC — U5 — AM335X_LCD_VSYNC 9
[LCD_HSYNC/GPMC_A9//PR1_EDIO_DATA_IN3/PR1_EDIO_DATA_OUT3/PR1_PRU1_PRU_R30_9/PR1_PRU1_PRU_R31_9/GPIO2_23] LCD_HSYNC — R5 — AM335X_LCD_HSYNC 9
[LCD_AC_BIAS_EN/GPMC_A11/PR1_MII1_CRS/PR1_EDIO_DATA_IN5/PR1_EDIO_DATA_OUT5/PR1_PRU1_PRU_R30_11/PR1_PRU1_PRU_R31_11/GPIO2_25] LCD_AC_BIAS_EN — R6 — AM335X_LCD_AC_BIAS_EN 9

VDDSHV6
R48 10K

[MCASP0_AHCLKX/EQEP0_STROBE/MCASP0_AXR3/MCASP1_AXR1/EMU4/PR1_PRU0_PRU_R30_7/PR1_PRU0_PRU_R31_7/GPIO3_21] MCASP0_AHCLKX — A14
[MCASP0_ACLKX/EHRPWM0A//SPI1_SCLK/MMC0_SDCD/PR1_PRU0_PRU_R30_0/PR1_PRU0_PRU_R31_0/GPIO3_14] MCASP0_ACLKX — A13
[MCASP0_FSX/EHRPWM0B//SPI1_D0/MMC1_SDCD/PR1_PRU0_PRU_R30_1/PR1_PRU0_PRU_R31_1/GPIO3_15] MCASP0_FSX — B13
[MCASP0_AXR0/EHRPWM0_TRIPZONE_INPUT//SPI1_D1/MMC2_SDCD/PR1_PRU0_PRU_R30_2/PR1_PRU0_PRU_R31_2/GPIO3_16] MCASP0_AXR0 — D12
[MCASP0_AHCLKR/EHRPWM0_SYNCI_O/MCASP0_AXR2/SPI1_CS0/ECAP2_IN_PWM2_OUT/PR1_PRU0_PRU_R30_3/PR1_PRU0_PRU_R31_3/GPIO3_17] MCASP0_AHCLKR — C12
[MCASP0_ACLKR/EQEP0A_IN/MCASP0_AXR2/MCASP1_ACLKX/MMC0_SDWP/PR1_PRU0_PRU_R30_4/PR1_PRU0_PRU_R31_4/GPIO3_18] MCASP0_ACLKR — B12
[MCASP0_FSR/EQEP0B_IN/MCASP0_AXR3/MCASP1_FSX/EMU2/PR1_PRU0_PRU_R30_5/PR1_PRU0_PRU_R31_5/GPIO3_19] MCASP0_FSR — C13
[MCASP0_AXR1/EQEP0_INDEX//MCASP1_AXR0/EMU3/PR1_PRU0_PRU_R30_6/PR1_PRU0_PRU_R31_6/GPIO3_20] MCASP0_AXR1 — D13

GPIO3_15 — AM335X_USB1_OC 6
GPIO3_16 — AM335X_LCD_DISEN 8
GPIO3_17 — LCD_BACKLIGHT_PWM 8
GPIO3_18 — LCD_BACKLIGHT_ENBL 8

R54 10K KEEP PULLDOWN UNTIL CONFIRMED DISPLAY DOESN'T NEED IT.

DGND

RTC

CHANGE TO SCHOTTKY DIODE?
BUT DON'T WANT HIGH LEAKAGE.

ISSUE: Nathan found that diode is backwards.
Layout/schematic done by Alex.
NEED TO FIX IN LAYOUT FOR P2.0
Grabbed the correct part from VOLGA WET and copied it here.
NEED TO ENSURE LAYOUT IS FIXED!
CAH 6/15/2015

+5V
R150 1.5K
R74 1K
D6 MMBD914
R73 4.75K
CR1 +3.1V BATT
C83 0.1uF
DGND

U17 PCF2123
3 SPI0_SCK — SCL
3 SPI0_SD0 — SDI
3 SPI0_SD1 — SDO
3 SPI0_CS0 — CE
CLKOE
VDD
OSC1
OSC0
CLKOUT
INT
NC_1
NC_2
TEST
GND

FSM 327
Y3

R72 100K
R149 100K

SPI CONNECTED PER AM3352 TECH REF MANUAL PAGE 4143.

VDDSHV6
R71 100K
VAUX2_3.3V 2,4,5,6,7,8

OPEN DRAIN INTERRUPT PIN CAN BE USED TO GENERATE A WAKE-UP SIGNAL ON AN INTERRUPT PIN (EXT_WAKEUP??).

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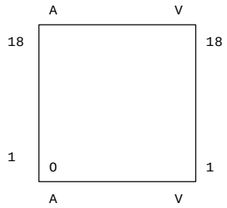

DDR3 HAS ON-DIE CAPACITORS, GETS .1uF CAPS ON BOARD.
THESE ARE 0201 SIZE.

AM335X

15mm x 15mm Package

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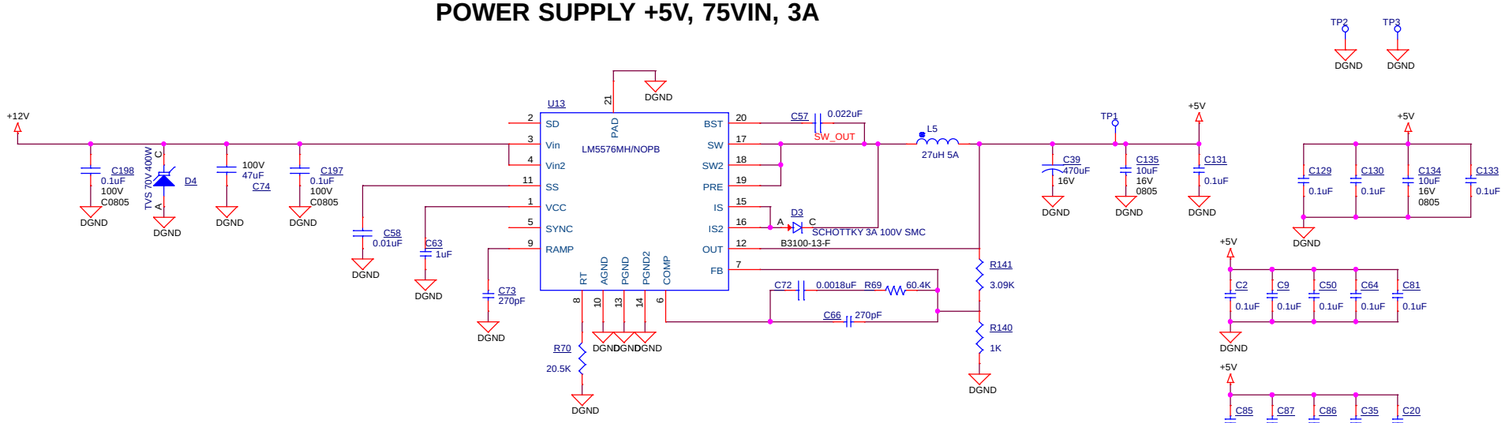
POWER SUPPLY +5V, 75VIN, 3A

POWER INPUT
+12V NOMINAL, 67V MAX.



HDS SAYS WE WILL USE RESET CKT AND A GPIO PIN AS A WATCHDOG TIMER.

```
TPS65910 Power Supply  AM335x Power Rail  Voltage
VAUX2 (300mA)  VDDSHV1, 3, 5,6 (500mA)  3.3V (rails that are 3.3V)
VDIG1 (300mA)  VDDSHV1, 3, 5, 6 (500mA)  1.8V (rails that are 1.8V)
VMMC (300mA)  VDDSHV4 (60mA) & VDDSHV2  1.8V/3.3V
VDD2 SMPS (1500mA)  VDD_CORE (1000mA)  1.1V
VDD1 SMPS (1500mA)  VDD_MPU (1500mA)  1.2V
No supply needed  VDD_RTC  1.1V
VRTC  VDDS_RTC (10mA)  1.8V
VIO_SMPS (1000mA)  VDDS_DDR (200mA)  1.8V (or 1.5V for DDR3)
VIO_SMPS (1000mA)  VREFSSTL (10mA)  0.9V or 0.75V
VDAC (150mA)  VDDS (100mA)  1.8V
VDIG2 (300mA)  VDDS_SRAM_CORE_BG
(40mA)||1.8V

VDIG2 (300mA)  VDDS_SRAM_MPU_BB (40mA)  1.8V
VDIG2 (300mA)  VDDS_PLL_DDR (25mA)  1.8V
VDIG2 (300mA)  VDDS_PLL_CORE_LCD (25mA)  1.8V
VDIG2 (300mA)  VDDS_PLL_MPU (25mA)  1.8V
VDIG2 (300mA)  VDDS_OSC (10mA)  1.8V
VAUX1 (300mA)  VDDA1P8V_USB0/1 (50mA)  1.8V
VAUX33 (150mA)  VDDA3P3V_USB0/1 (10mA)  3.3V
VAUX33 (150mA)  USB_VBUS0/1  3.3V
VPLL (50mA)  VDDA_ADC  1.8V
VDD3 SMPS (100mA)  Not Used  -
VIO_SMPS (1000mA)  DDR2 SDRAM (320mA)  1.8V

Table 3: AM335x Power supplies from TPS65910A
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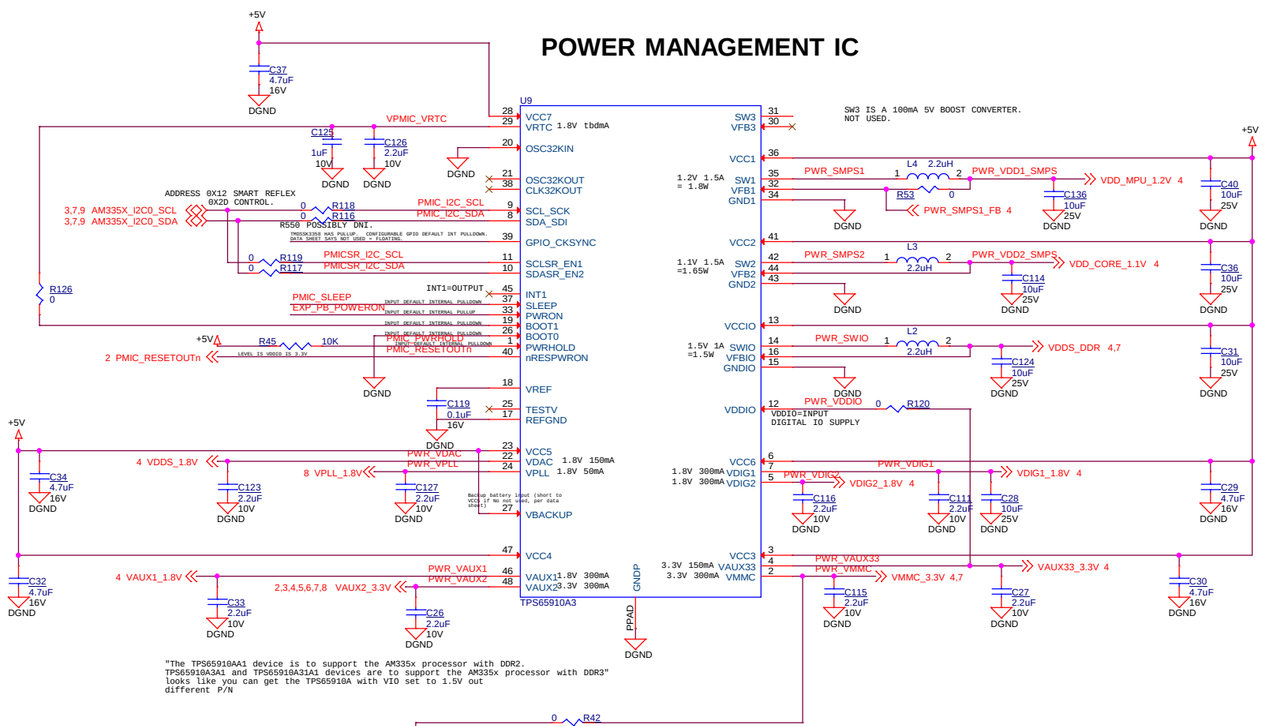
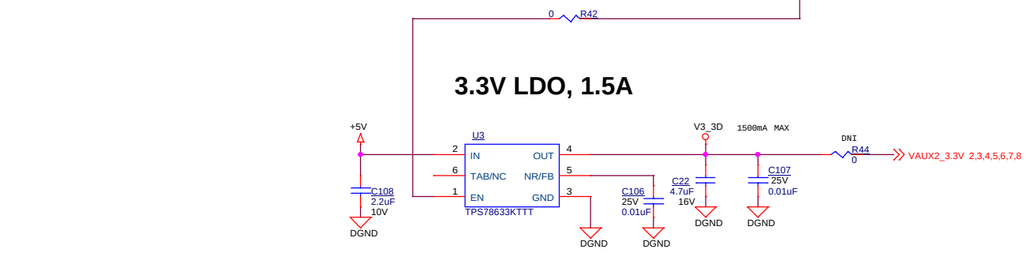
POWER MANAGEMENT IC

HDS SAYS WE WILL SEND POWER GOOD SIGNAL TO PROCESSOR. THIS IS THE nRESPWRON SIGNAL, WHICH RESETS THE PROCESSOR WHEN LOW.





CAN THE TPS65910 HANDLE THIS POWER REQ?

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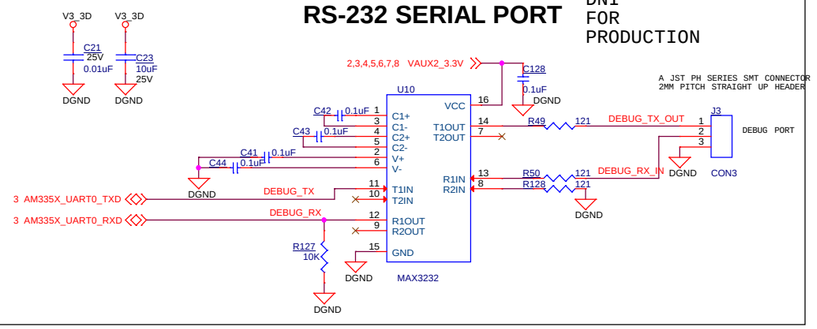
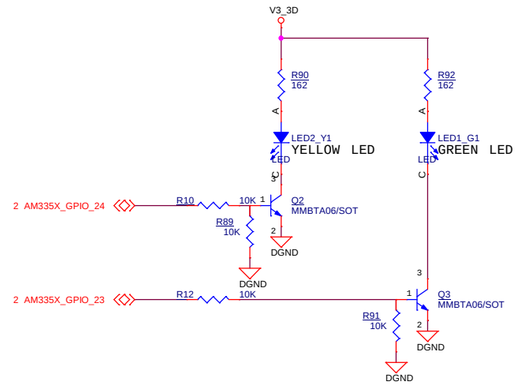
RS-232 SERIAL PORT

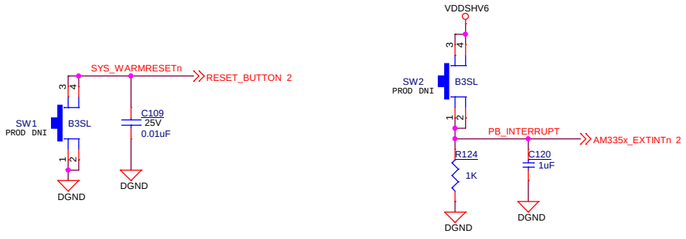
DNI
FOR
PRODUCTION



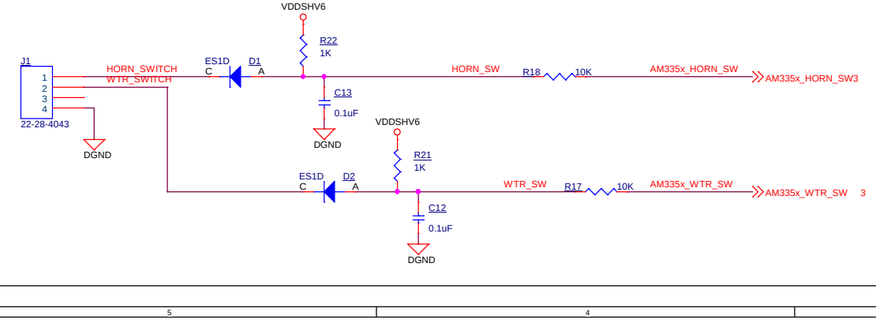
USER LED'S



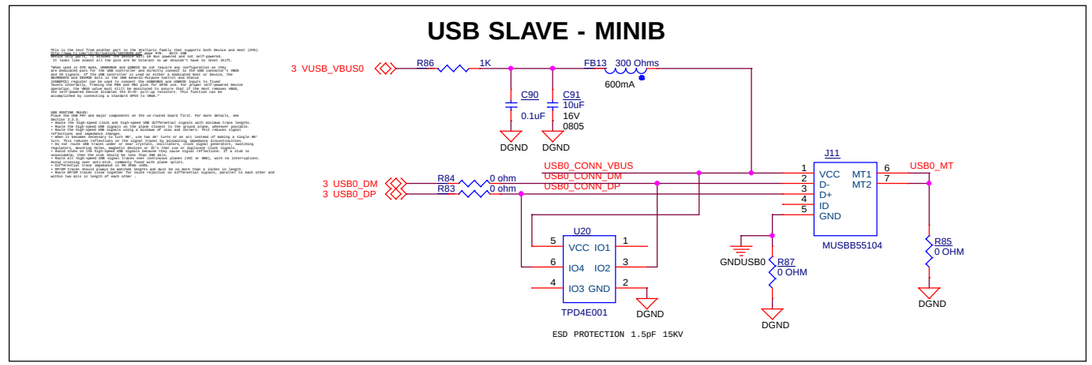
USER RESET/INTERRUPT SWITCHES



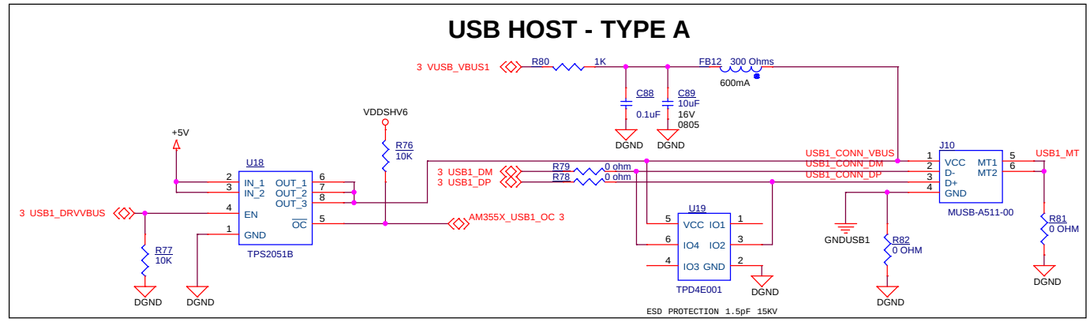
HORN / POWER ON-OFF SWITCHES



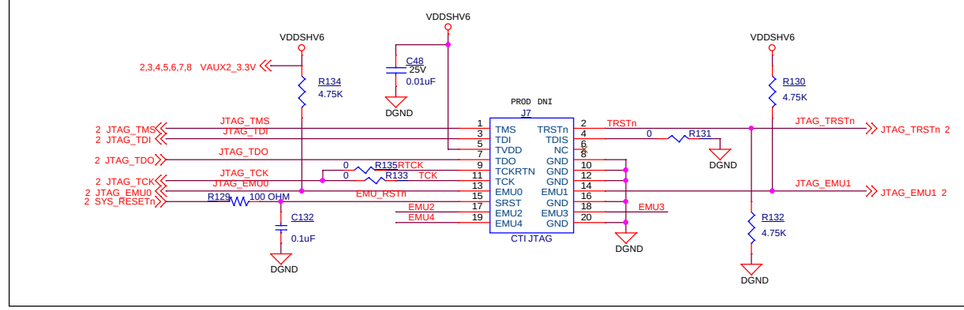
USB SLAVE - MINIB



USB HOST - TYPE A

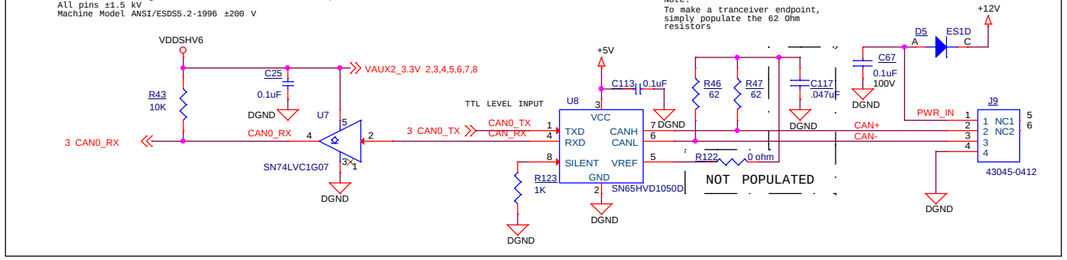


JTAG CONNECTOR



CAN INTERFACE

ELECTROSTATIC DISCHARGE PROTECTION
over operating free-air temperature range
PARAMETER TEST CONDITIONS VALUE
IEC Contact Discharge IEC 61000-4-2 Bus terminals vs GND ±6 kV
Human Body Model JEDEC Standard 22,Test Method A114-C.01 Bus terminals vs GND ±8 kV
All pins ±4kV
Field-Induced-Charged Device Model JEDEC Standard 22,Test Method C101
All pins ±1.5 kV
Machine Model ANSI/ESDS5.2-1996 ±200 V



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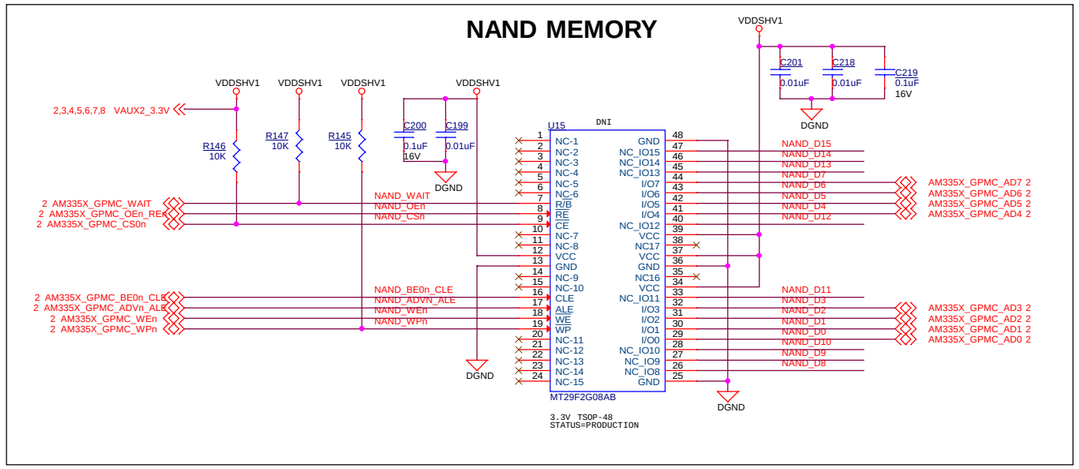
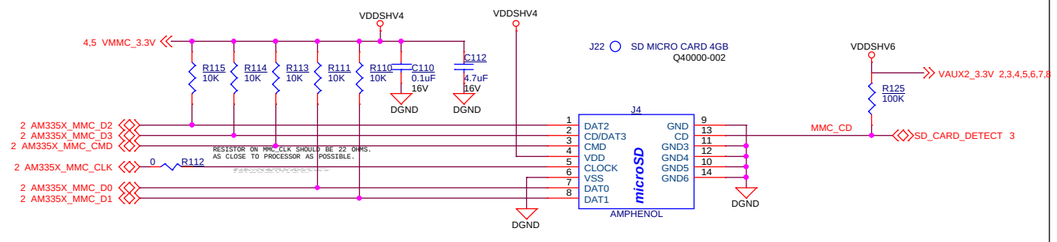
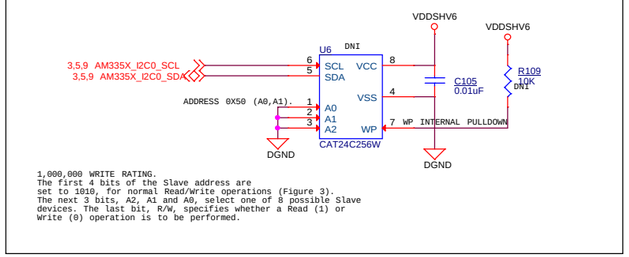
NAND MEMORY



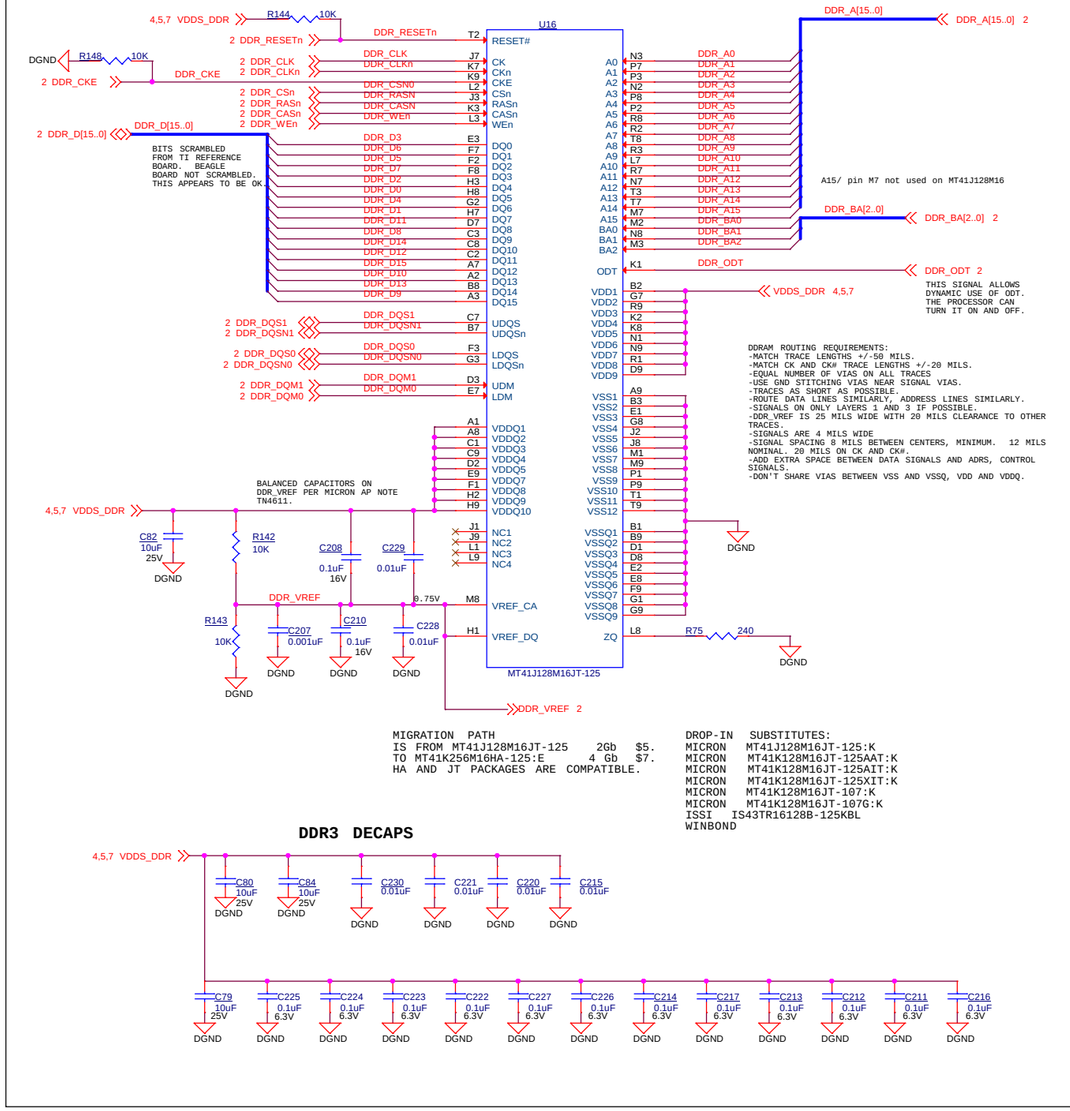
MICRO SD CONNECTOR



ID MEMORY 256Kb DNI



DDR3 SDRAM



MIGRATION PATH
IS FROM MT41J128M16JT-125 2Gb $5.
TO MT41K256M16HA-125:E 4 Gb $7.
HA AND JT PACKAGES ARE COMPATIBLE.

DROP-IN SUBSTITUTES:
MICRON MT41J128M16JT-125:K
MICRON MT41K128M16JT-125AAT:K
MICRON MT41K128M16JT-125AIT:K
MICRON MT41K128M16JT-125XIT:K
MICRON MT41K128M16JT-107:K
MICRON MT41K128M16JT-107G:K
ISSI IS43TR16128B-125KBL
WINBOND

DDR3 DECAPS

DDR3 MEMORY DESIGN TAKEN FROM BEAGLE BONE BLACK BOARD.

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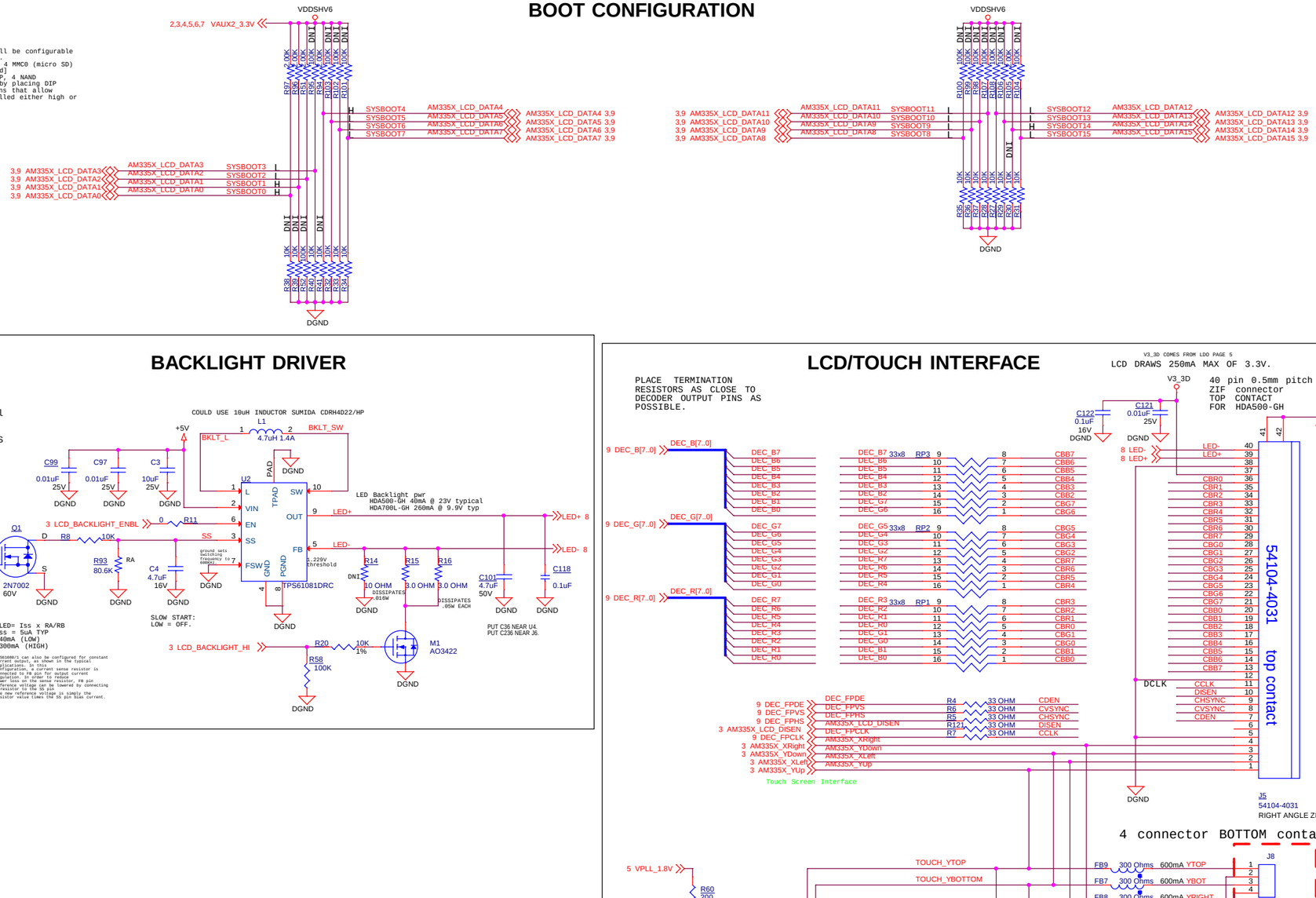
BOOT CONFIGURATION

The boot sequence shall be configurable between two sequences.
1 USB, 2 NAND, 3 SPI, 4 MMC0 (micro SD)
[NOTE: SPI is not used]
1 EMAC1, 2 MMC0, 3 XIP, 4 NAND
This may be achieved by placing DIP switches or jumper pins that allow SYSBOOT[3:2] to be pulled either high or low.



BACKLIGHT DRIVER

The backlight brightness shall be controllable from the processor via a PWM signal.
R204 SETS BACKLIGHT BRIGHTNESS RANGE. MAY NEED ADJUSTMENT.

LCD/TOUCH INTERFACE

PLACE TERMINATION RESISTORS AS CLOSE TO DECODER OUTPUT PINS AS POSSIBLE.

V3_3D COMES FROM LDO PAGE 5
LCD DRAWS 250mA MAX OF 3.3V.

40 pin 0.5mm pitch ZIF connector TOP CONTACT FOR HDA500-GH

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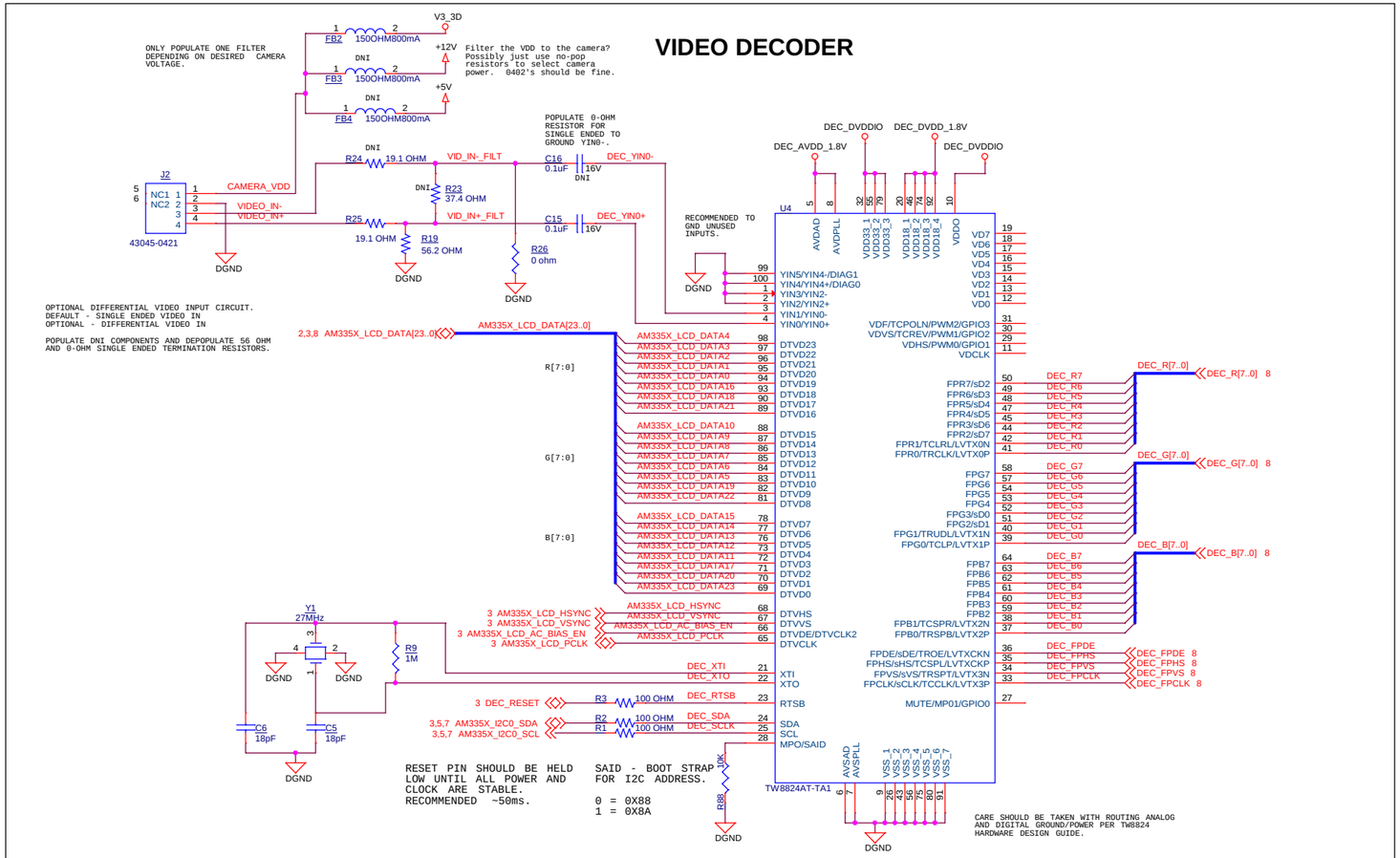
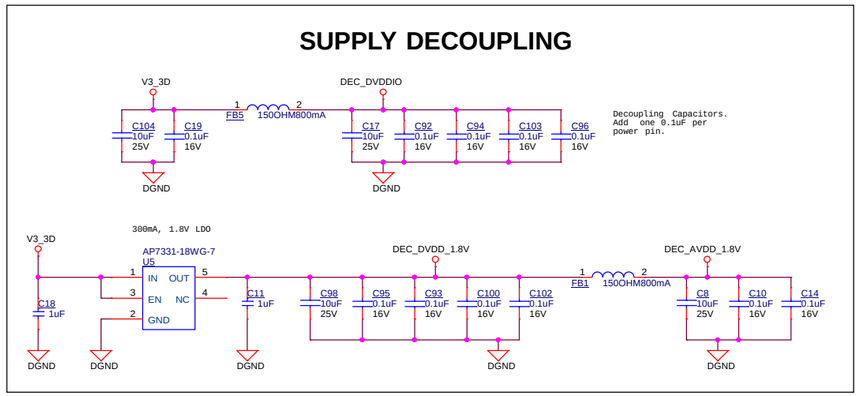
VIDEO DECODER



SUPPLY DECOUPLING



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