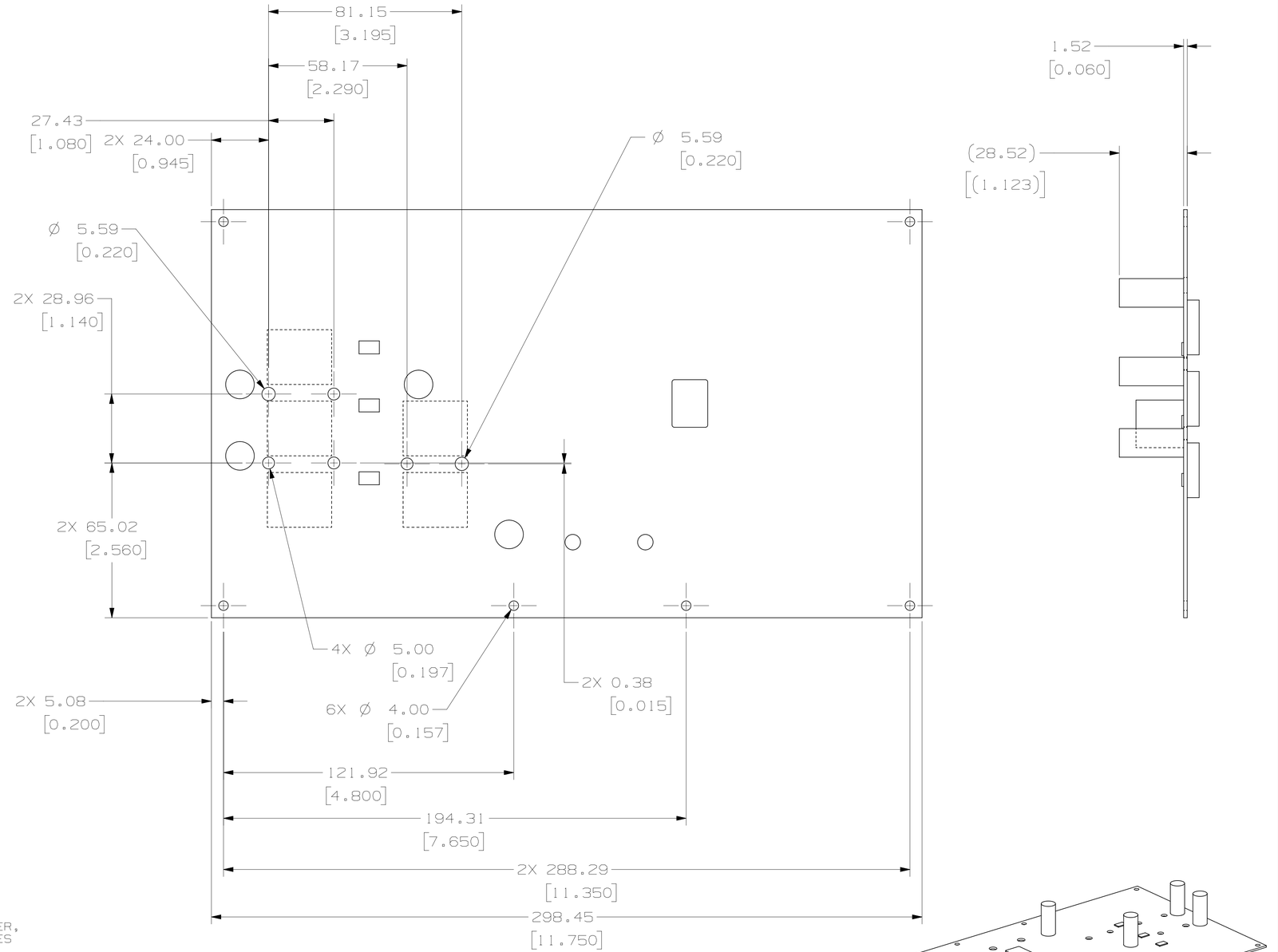
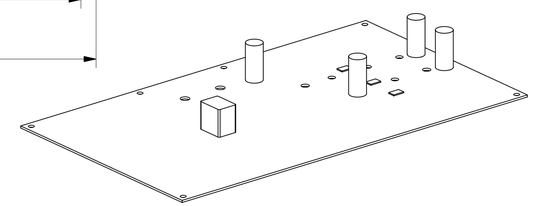
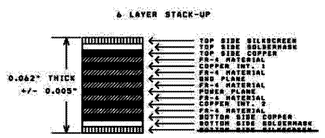
NOTES:
1) BUILD USING QPL BILL OF MATERIAL BOM1054014rvH.
2) WORKMANSHIP STANDARD, SOLDERING AND ELECTRICAL CONNECTIONS PER: IPC-J-STD-001D OR LATEST REVISION.
3) THIS PRINTED CIRCUIT BOARD ASSEMBLY IS NOT A PURCHASED PART. IT IS USED IN ASSEMBLY 1076761, WHICH IS A PURCHASED PART.
4) APPLY TWO LABELS IN DESIGNATED LOCATION WITH THE FOLLOWING INFORMATION:
   LABEL #1: TENNANT'S QPL BOM PART # WITH CURRENT ALPHA REVISION (EX: BOM1054014rvG).
   LABEL #2: MANUFACTURER SERIAL NUMBER WITH BAR CODE FOR TRACEABILITY. (SEE PAGE 2 OF 2 FOR LABEL LOCATION.)
5) CONFORMAL COAT AS PER INSTRUCTIONS ON PAGE 2 OF 2.
6) HARDWARE (Q17006-004, Q17005-006 AND Q17007-003) IS USED TO HOLD CONNECTOR J5 TO THE PCB. THE HEADS OF THE BOLTS TO BE ON THE BOTTOM SIDE OF THE PCB.
7) ICT AND FUNCTIONAL TESTING REQUIRED.
8) TO LOCATE THE BILL OF MATERIAL FOR THIS BOARD, FOLLOW THE STEPS LISTED
   A. GO TO "http://tennantengineering.com"
   B. CLICK ON TEXT, "qpl documentation"
   C. CLICK ON TEXT, "bills of materials"
   D. CLICK ON THE APPROPRIATE TEXT, "1054014...QUANTUM CONTROLLER"
   E. UNDER "to download/view files":
      1. ENTER PASSWORD (SUPPLIED BY TENNANT)
      2. CLICK ON BUTTON LABLED "list filenames"
   F. CLICK ON BOM1054014rvH.XLS.
   G. DOWNLOAD REQUIRED FILES AS SPECIFIED IN THE BOM
9) APPLY NON-CORROSIVE PCB SAFE RTV TO THE FOLLOWING COMPONENTS FOR VIBRATION PROTECTION: BASE OF COMPACITORS C205, C206, C207 C208, C209, C84, C92, C88, AND INDUCTORS L3 AND L4
10) ASSEMBLY TO BE MANUFACTURED PER RoHS/LEAD FREE STANDARDS.



PCB MANUFACTURING NOTES:
1) MATERIAL SELECTION: FR-4 UL RECOGNIZED ZPMV2 MIN. 130C FLAME CLASS V-0 OR BETTER, .062 +/-.007 THICK. MATERIAL PER IPC-4101, 2OZ. COPPER MIN.. SOLDERABLE SURFACES TO BE ENIG(ELECTROLESS NICKEL IMMERSION GOLD).
2) SOLDER RESIST: THE USE OF SOLDER RESIST COATING SHALL BE IN ACCORDANCE WITH THE REQUIREMENTS OF IPC-SM-840. ALL SOLDERABLE SURFACES ARE TO BE FREE OF SOLDER RESIST. COLOR - GREEN. USE LIQUID PHOTOIMAGEABLE RESIST.
3) SILKSCREEN: USE WHITE NON-CONDUCTIVE INK. ALL COMPONENT AND TEST POINT LANDS ARE TO BE FREE OF INK.
4) MANUFACTURER'S IDENTIFICATION: ADD IN ETCH OR TO SILKSCREEN.
5) ELECTRICAL BARE BOARD TEST REQUIRED.
6) DRILL SIZES ARE FINISHED SIZE AFTER PLATING.
7) FABRICATE TO MEET EU RoHS DIRECTIVE.
8) PCB MUST HAVE UL 94V-0 RATING MARKED ON EACH SIDE.
9) MAX WARP AND TWIST NOT TO EXCEED 0.010 PER LINEAR INCH.
10) PCB CORNER RADIUS: N/A.
11) MIN. ANNULAR RING: -.003 MIN PLATED HOLE WALL THICKNESS .001.
12) DIMENSION TOL: XX +/-0.010 XXX +/-0.005.
13) USE GERBER FILE DATA TO ESTABLISH DRILL COUNTS.
14) COPPER THIEVING OF THE SIGNAL LAYERS IS ALLOWED, SPACING TO ANY EXISTING BOARD FEATURE TO BE 0.060 MINIMUM.



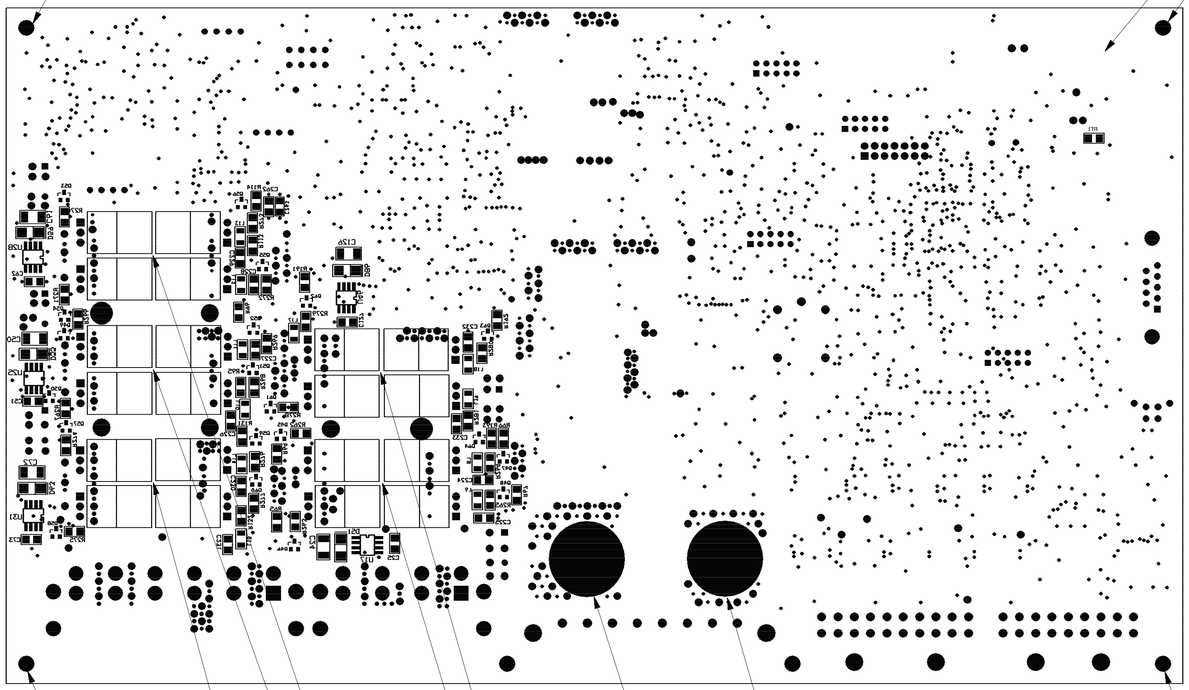


ECO CONSULTATION

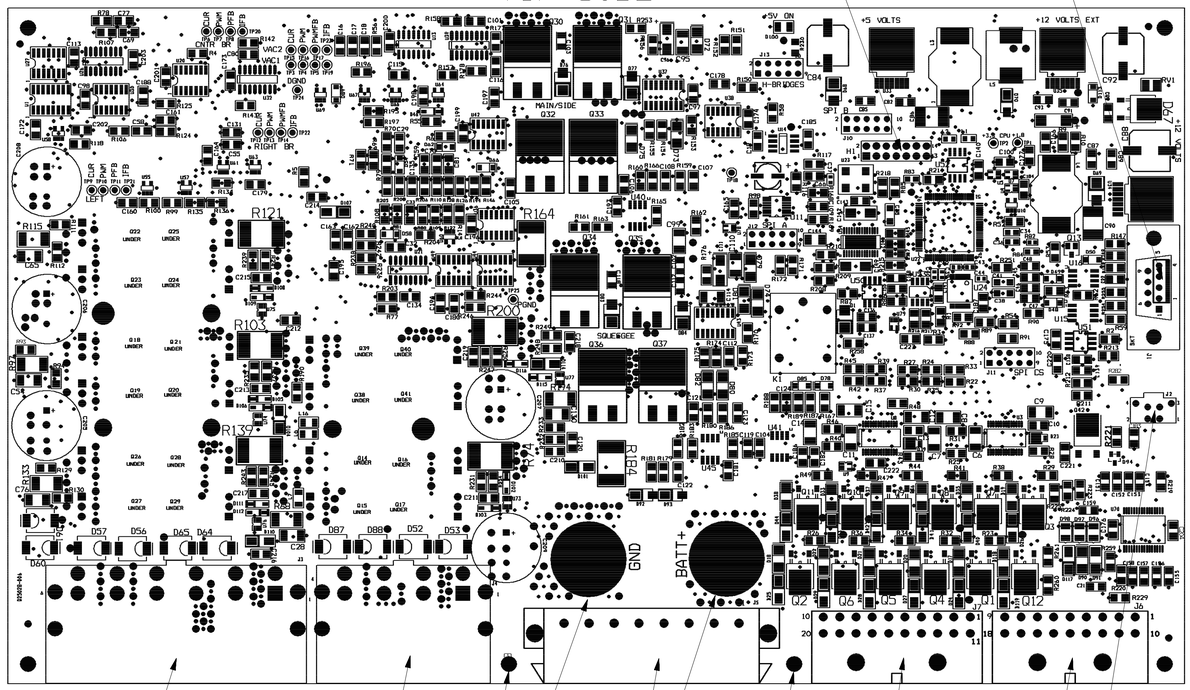
MATERIAL SPECIFICATIONS: NOTED		PAINT - COLOR NONE		04		JPH	01/08/2020
OTHER TREATMENTS AND FINISHES NONE		PAINT - GLOSS	PAINT - PERFORMANCE / PAINT - ACCEPTANCE	REV	ECO	BY	DATE
SCALE: 1:1	DO NOT SCALE DWG	TOLERANCES UNLESS OTHERWISE SPECIFIED		GENERAL NOTES: PRIMARY DIMENSIONS ARE METRIC, SECONDARY DIMENSIONS WITH BRACKETS ARE INCH. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE AFTER TREATMENTS AND FINISHES.	TENNANT
DWN: LARRY JENSEN 01/14/2010		METRIC TOLERANCES	INCH EQUIVALENT		
MDR: JIM HANSEN 02/25/2010		LINEAR ±0.127	±.005	PROPRIETARY INFORMATION: MAY NOT BE REPRODUCED OR DISCLOSED TO OTHERS WITHOUT WRITTEN PERMISSION OF TENNANT COMPANY.	
DES: JOHN HAEG 01/14/2010		SLOT WIDTH ±0.076	±.003		
		HOLE DIA ±0.076	±.003		
		ANGULAR ±2°			
		MACH SURFACES 3.2 RMS	125 RMS		
PART NAME: CIRCUITBOARD [T16]		SHEET 1 OF 2		DWG SIZE: D	PART NUMBER: 1054014

LABELS LOCATED HERE.
REFER TO NOTE #4 ON PAGE 1 OF 2.

BOTTOM SIDE



TOP SIDE



CONFORMAL COATING NOTES:
1) CONFORMAL COATING MATERIAL (TWO OPTIONS):
   A) TEMPO CHEMICALS CO. LTD, #TS1066@.
   APPLIED COATING TO BE 130-1000(MIC) THICK.
   B) DYMAX CORP. #9-20557.
   APPLIED COATING TO BE 91-112(MIC) THICK.
2) MASK OFF THE FOLLOWING AREAS ON THE TOP SIDE OF THE ASSEMBLY:
- CONNECTORS J1, J2, J3, J4, J5, J6, J7, J10 AND JTAG PROGRAMMING PORT H1, SO CONFROMAL COATING DOES NOT WICK UP THE CONNECTOR LEADS.
- PADS FOR BATT+ AND GND STANDOFFS.
3) MASK OFF THE FOLLOWING AREAS ON THE BOTTOM SIDE OF THE ASSEMBLY:
- PADS FOR BATT+ AND GND STANDOFFS.
- TRANSISTOR BOTTOM SURFACES FOR FOR ALL (20) POWER MOSFETS, SO THE TRANSISTORS WILL HAVE GOOD THERMAL CONDUCTION WITH THE HEATSINK THAT IS GOING TO BE APPLIED.
4) ALL SIX OF THE ASSEMBLY MOUNTING HOLES SHOULD BE MASKED OFF.
5) CONNECTORS J10, J11 AND J13 ARE NOT POPULATED, AND DO NOT REQUIRE SOLDER MASK.

REV-04 CHANGES:
1) CORRECTED QPL BOM TO BOM10544rvH
2) UPDATED THE REFERENCE TOP ASSEMBLY CIRCUIT BOARD TO 1076761.

ECO CONSULTATION

MATERIAL SPECIFICATIONS: NOTED	PAINT - COLOR NONE			04	JPH 01/08/2020
OTHER TREATMENTS AND FINISHES NONE	PAINT - GLOSS	PAINT - PERFORMANCE	PAINT - ACCEPTANCE	REV ECO	BY DATE

SCALE: NONE — DO NOT SCALE DWG

DWN: LARRY JENSEN 01/14/2010
MDR: JIM HANSEN 02/25/2010
DES: JOHN HAEG 01/14/2010

PART NAME: CIRCUITBOARD [T16]

TOLERANCES UNLESS OTHERWISE SPECIFIED

METRIC TOLERANCES		INCH EQUIVALENT
LINEAR	±0.75	±.030
SLOT WIDTH	±0.25	±.010
HOLE DIA	±0.25	±.010
ANGULAR	±2°	
MACH SURFACES	3.2 RMS	125 RMS

GENERAL NOTES
PRIMARY DIMENSIONS ARE METRIC, SECONDARY DIMENSIONS WITH BRACKETS ARE INCH. UNLESS OTHERWISE SPECIFIED ALL DIMENSIONS ARE AFTER TREATMENTS AND FINISHES.

SHEET 2 OF 2

TENNANT

DWG D SIZE — PART NUMBER 1054014